

# TurboCATS II – 700

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**700 MHz DDR1/DDR2 Single-Site Memory Test System**



**USER'S MANUAL**


# **TCII - 700 User's Manual**

Release 2.1 - April 2006

## **Triad Spectrum, Inc.**

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## TurboCATS™ II – 700 Memory Test System Overview

The purpose of this manual is to get you acquainted with our TurboCATS II – 700MHz memory tester. It combines the power, speed and accuracy of our multi-site TurboCATS III tester and the compact design of the previous generation of single-site TurboCATS II series.

TurboCATS II - 700 is designed for testing today's DDR1/DDR2 memory components and modules of any size and configuration up to 700 MHz.

TurboCATS II - 700 achieves highly accurate test results by providing the user with over 35 AC/DC complex parametric test patterns and by using the super-fast, high bandwidth bus for executing all test algorithms. The user can vary the timing parameters for test patterns at 50ps resolution to match Jedec/Intel specifications. Loading effects and noise are also simulated with the "dual socket" test condition, which in addition to the features mentioned above allows us to say that the accuracy of the TurboCATS™ II - 700 test results is over 99%.

The TurboCATS II – 700 memory test system uses the specialized software program that provides a friendly graphical user interface and easy to read error displays (both text and graphical). It gives the user an ability to store test results in the special database and then create report files by searching it. For testing good-die and fall-out ICs, it has an optional feature to perform I/O and address sorting and binning as a part of a single test. The communication between the PC and tester is accomplished via a single USB link. You can connect it to any PC of your own (Win2000 OS required) – we provide the software together with the tester, and all software upgrades (new versions) after that are yours for free!

## Using This Manual

This User's Manual is designed to familiarize you with all of the functions mentioned above, so that you can use the TurboCATS II – 700 Memory Test System to its fullest potential. This Manual is intended for both first-time and experienced users who want to learn about the tester's features and operation, have questions on how to use certain functions, or need to upgrade their system. It is assumed that the user has a basic working knowledge of memory devices. Although the TurboCATS II – 700 software that accompanies this tester is very intuitive, Triad Spectrum, Inc. recommends the user to look through the entire manual prior to operating the tester – system malfunction as a result of user's negligence is not covered under our warranty.



**CAUTION:** Please make sure you read **Chapter 2** in order to correctly setup the system before attempting to apply power to the tester.

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# Chapter 1

## System Architecture and Specifications

### 1-1 Hardware Terminology

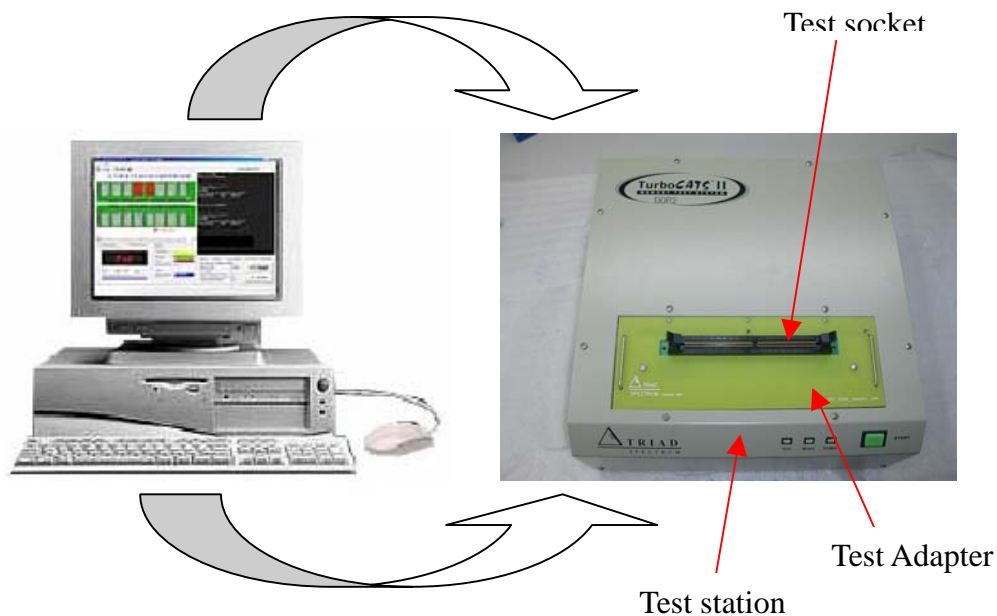


Figure 1-1. TurboCATS™II – 700 Memory Test System

The following terminology is frequently used in this User's Manual when describing the TurboCATS II – 700 Memory Test System:

<b>TCII - 700</b>	is the short name for TurboCATS II – 700MHz Memory Test System
<b>Test Station or Test Header</b>	is the mechanical body of the test system, which holds a Base board and a FPGA board inside
<b>Base Board</b>	is the main PCB which contains MCU and components that generates algorithms, processes results and provides DC testing, etc.
<b>FPGA Board</b>	contains FPGA's IC which generates clock signals and provides AC testing
<b>Passive Adapter</b>	is designed for the connection interface from a FPGA board to the test socket. It also contains analog switch to change the channels
<b>Test Socket</b>	is used to plug in the DUT(Device Under Test).

The tester comes with a standard 240-pin DDR2 DIMM socket and a passive adapter with a 200-pin DDR2 SODIMM, 184-pin DDR1 DIMM,



200-pin DDR1 SODIMM sockets are optically available

Table 1-1 describing the TurboCATS II – 700 Memory Test System

## 1-2 Current System Specifications

<b>Memory Types Supported</b>	DDR1 and DDR2 SDRAM
<b>Module Standards Supported</b>	DDR1: PC1600 (100MHz), PC1700 (110MHz), PC2100 (133MHz), PC2200 (140MHz), PC2700 (166MHz), PC2800 (180MHz), PC3200 (200MHz), PC3500 (220MHz),  DDR2: PC3200 (200MHz), PC3500 (220MHz), PC4300 (266MHz), PC4500 (280MHz), PC5300 (333MHz), PC5600 (350MHz)
<b>Module Types Supported</b>	184 pin DDR1 DIMM, 200 pin DDR1 SODIMM 240 pin DDR2 DIMM, 200 pin DDR2 SODIMM (adapter available)
<b>Module Configuration</b>	Unbuffered & Registered
<b>Test Frequency</b>	DDR1: 100MHz to 220MHz  DDR2: 200MHz to 350MHz
<b>Switching Data Rate</b>	400Mb/sec/pin to 700Mb/sec/pin
<b>I/O Interface</b>	SSTL_18 (1.8V ± 0.1V Power Supply)
<b>Address Generation</b>	14X + 11Y + 3Z (X=Rows, Y=Columns, Z=BS)
<b>Data Width</b>	72 bits
<b>Control Lines</b>	Unbuffered: 2-CS, 1-RAS, 1-CAS, 1-WE, 8 differential DQS, 8-DM  Registered: 2-CS, 1-RAS, 1-CAS, 1-WE, 9 differential DQS, 9-DM
<b>DUT clocks</b>	3 pairs of differential signals

<b>Variable Timing Edges</b>	<p>tSU/tHD, tDQSS, tDS/DH, tRP, tRRP, tRCD, tAL, tCL, tWL, tRL, tWR @ 50ps increments</p> <p>tSU/tHD: Address &amp; controls setup and hold time  tDQSS: DQSS minimum and maximum time  tDS/tDH : Data setup and hold time referred to DQS edges  tRP : precharge command period  tRCD : active to read or write delay  tAL : the time of additive latency  tCL : clock low-level width  tDQS : DQS lines minimum/maximum time  tWR : Write recovery time</p>
<b>Variable Test Voltage</b>	<p>Vdd : 1.6V to 2.0V, 0.01V increments @ 5A, +/- 2% accuracy  Vref : 1/2 of Vdd, +/- 5% accuracy (tracking with Vdd)  Vtt : 1/2 of Vdd, +/- 5% accuracy (tracking with Vdd)  Vspd : 1.5V, 1.8V &amp; 2.5V @ 5A, +/- 1% accuracy</p>
<b>Icc Measurements</b>	<p>Operating (Single and Burst Read/Write cycles), Auto-Refresh, Standby &amp; Self-Refresh currents</p> <p>Range 1: 0mA – 50mA @ 100uA resolution, +/- 100uA accuracy  Range 2: 50mA – 100mA @ 1mA resolution, +/- 1mA accuracy  Range 3: 100mA – 700mA @ 5mA resolution, +/- 5mA accuracy  Range 4: 700mA – 5A @ 50mA resolution, +/- 50mA accuracy</p>
<b>Leakage Measurements (per pin)</b>	<p>Range 1: 0uA – 10uA, +/- 1uA accuracy  Range 2: 10uA – 100uA, +/- 2uA accuracy  Range 3: 100uA – 1mA, +/- 25uA accuracy  Range 4: 1mA – 4mA, +/- 450uA accuracy</p>
<b>AC Tests Available</b>	<p>Electrical: Open/Shorts, Auto-Refresh, Self-Refresh, Data Retention, Volatility, Vcc_RW  Marching: Burst Scan RW, Burst Scan Toggle, March 1/0, MAT+, MAT++, March A, March B, March C, March C-, March CR, March G, March LA, March LR, March U, March UD, March UR, March Y, PMOVI, PMOVIR  Base Cell: Checkerboard, Memory Scan  Repetitive: Ham Rd, Ham_Wr</p>
<b>SPD EEPROM Operations</b>	<p>SPD Read, Program, Edit, Test, Serialization, Software/Hardware Write-Protect, Slot Test of all SPD lines</p>
<b>Minimum PC requirements (PC not provided)</b>	<p>Windows 2000 operating system, Pentium IV, 40GB HD, 256MB Memory, VGA resolution (1024X768), CDROM drive, floppy drive, Advanced setting under display of “large fonts”, minimum one USB slot  (communication between PC and tester station via a single USB link)</p> <ul style="list-style-type: none"> <li>REMARK: User needs to provide monitor, mouse, keyboard &amp; memory module of his own</li> </ul>
<b>Test Station Weight</b>	<p>19 lb (8.6 kg)</p>
<b>Test Station Size (fully assembled)</b>	<p>330mm(W) X 325mm(L) X 140mm(H)</p>
<b>AC Power Source</b>	<p>110 AC – 240 AC, 50/60 Hz</p>

<b>Operating Temperature</b>	40° - 90° F (4° - 32° C)
<b>Operating Humidity</b>	20% - 55% (non-condensing)

Table 1-2 current system specifications

## Chapter 2

# System Setup

### 2-1 List of Materials

The following items are included with your TurboCATS II-700 Memory Test System shipment:

- A. one (1) test station, which holds one (1) Base board and (1) FPGA board
- B. one (1) passive test adapter with a standard 240-pin DDR2 dual test socket
- C. one (1) tester power cable
- D. one (1) USB cable
- E. CD-ROM containing the most current versions of the TCII-700 Software program, the Driver files, the TCII-700 User's Manual and Installation Instructions in PDF format.



**NOTE:** If there are any items missing from the shipping carton according to your purchase order or the packing list, please contact your local Triad Spectrum representative or our factory immediately.



**NOTE:** You need to prepare your own PC (Win 2000 Operating System), monitor, keyboard, mouse and CD-ROM drive to work with the TCII-700 memory test system.

### 2-2 Hardware / Software Setup

Following instructions are listed precisely in sequential order. Please contact us if you have any questions or problems setting up your TCII-700 Memory Test System.

**STEP 1.** Prepare a workbench for the TurboCATS II - 700 Tester. Please ensure that the area is large enough to hold the test station (13.2"x13") and your monitor, and should be able to support their weight.

Place the test station on the workbench. Note that with shipping the test adapter is already plugged in. Therefore, please do not place the monitor on the top of the tester.

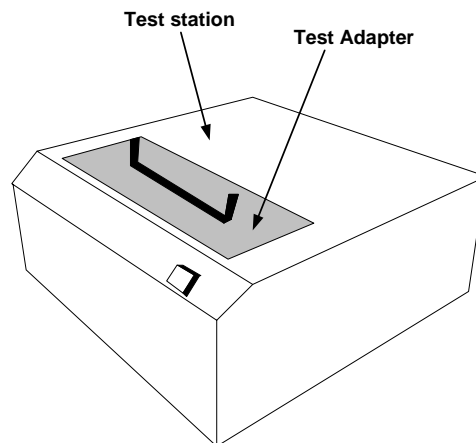


Figure 2-1. TurboCATS II – 700 System

**STEP 2.** Examine the location of each port on the test station as figure 2-2 below as a guide.

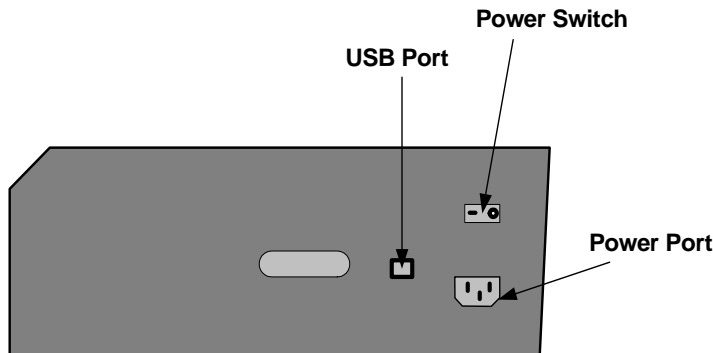


Figure 2-2. Right Panel of TCII-700 Test Station

<b>Tester Power Port</b>	The tester power cable (provided with the system) connects this port on the tester to the external power outlet. Any AC power supply ranging 110-240 V can be used.
<b>Tester Power Switch</b>	Left = ON, Right = OFF
<b>USB Port</b>	You need your own external PC to control the tester's operation. The USB cable included in the system connects this USB Port on the tester to the bottom USB slot (closest to the motherboard) on your PC.

**STEP 3.** Make sure the **Tester Power Switch** is in the OFF position. Connect the **Tester Power Port** and the external power outlet with the Tester Power Cable.

**STEP 4.** Make sure all the peripherals are plugged in (keyboard, mouse and monitor are necessary for using the TCII-700 Software Program), and your PC is powered up.

**STEP 5.** Connect your PC to the tester using the provided USB cable. Use the bottom USB slot (closest to the motherboard) on your PC.

Turn the **Tester Power Switch** ON.

When hooking up the system for the first time, there would be a pop up window message on the PC screen informing you that a new hardware is found and will prompt you for the system driver – please browse the file in the location that holds the provided driver files (folder '**TCII-700 Driver**' on the CD-ROM, for example). If you don't see the pop-up

message, please try plug to another USB slot on your PC.



**NOTE:** If you have problems installing driver files, you may be using an Operating System other than Windows 2000. Note that our TCII-700 Software Program was developed for Win2000 OS only.

**STEP 6.** Install the TurboCATS II – 700 Software program in your PC. Start by double-clicking on the **SETUP.EXE** application file (blue icon) in the '**Disk 1**' folder and follow the instructions.

It will automatically locate the TurboCATS II-700 software on your PC under the **C:\Program Files\TCII-700** directory. A shortcut to TurboCATS II-700 icon would also be created on your desktop. To run the TurboCATS II-700 Software Program, click on that icon.

## 2-3 General System Power-Up

**STEP 1.** To start with, make sure your PC is powered on. Also, make sure there is NO memory modules plugged into the test socket. Turn the **Tester Power Switch** ON. Wait for a couple of minutes for the tester to initialize: the Base board establishes communication with the PC – during this initialization you can observe all 3 green LEDs next to the **Start** button (at the front of the tester) flashing. Wait until all lights stop flashing before using the software and the tester.

**STEP 2.** Open the TCII-700 Software Program by double-clicking on its icon on the PC desktop screen. Watch the bottom left corner of the software Main Operating Screen – it will indicate whether the communication with the board has been established. The **Start** button (on the right bottom corner of the screen) will then be enabled and testing can be started then.

# Chapter 3

## Quick Start

This chapter contains a brief overview of the operating procedure to give reader a general idea of how the TurboCATS II - 700 memory tester is used and to familiarize you with our software terminology.

### 3-1 Software Terminology

<b>Software</b>	TCII-700 software program installed on the PC that controls the tester.
<b>Firmware</b>	File that was downloaded to the Baseboard and programmed in the memory.
<b>Test File</b>	File that defines the test procedure: contains information about device parameters, test patterns and SPD contents.
<b>Test List</b>	Contains a list of test patterns to run on the DUT. It is included in the Test File.
<b>Test Pattern</b>	One test, for example Checkerboard.

### 3-1 Operating Procedure Overview

Procedure given below will illustrate how to use TurboCATS II - 700 to test a module and program its SPD EEPROM based on a known good module. All the testing procedure steps given here will be described in much more detail in Chapter 4, so please refer to it if you have any questions about these operating instructions. For this example you need one 'golden' module (tested previously / known good and programmed with good SPD data) with x8 ICs and the same parameters as the other modules you want to test. First, set up the TCII-700 system following the procedure described in Chapter 2 and turn the tester on. Launch the TurboCATS II-700 software program. After the initialization PC screen, you will be directed to the Main Operating Screen. Only change the settings described in this procedure – leave the others as default, you will get acquainted with them later in Chapters 4 and 5.



**NOTE:** If anytime during the tester operation, the software pop-up message on the screen informs you of a failed USB communication, please close the software program, restart the tester, and then open the program again. If the problem persists, you may need to restart your PC to eliminate the glitch.

#### Use the known good module to create a Test File:

1. Insert a known good x8 module into the socket.
2. Click on the Edit Test File icon to enter the Test File screen for the DUT. Click on the Open **Test File** icon and select a Test file called **Template.tf** and checked the AutoID box that will automatically identify the device parameters of your module during testing. Back in the Test File screen (**Device** tab), select the appropriate **Module Type** field setting and the **Configuration** field to specify whether your module is unbuffered or registered. Press on the **Test List** tab, and select the correct frequency and CL settings for your module. Then press the **Exit** icon to get back to the Main Operating Screen.

3. In the Main Operating Screen, make sure that the name of the Test File displayed on the top of the screen is Template.tf. And also the tester is in **Connected** status (displayed at the bottom left corner of the screen). Press the **Start** button to run the test.
4. After the test is finished, the right side of the screen should now have the correct parameters of your module, identified by the Auto ID function you selected previously (**R/C/Bs** field displays the Number of Rows/ Number of Columns/ Number of Bank Select Lines on the module).
5. Click on the Edit Test File icon to get to the Test File screen again. The **Device** page (displayed first by default) now contains the correct parameters for your module. Press the Save Test File icon to save this Test File, enter Example1.tf in the File Name field, and press **SAVE**. Press the **Exit** icon to get back to the Main Operating Screen.

### Start testing the modules:

1. Insert the module you want to test /program into the test socket.
2. Click on the **Edit Test File** icon to enter the Test File screen for the DUT. Click on the Test File screen (**Device** tab), select the appropriate **Module Type** field setting, and also select the **Configuration** field to specify whether your module is unbuffered or registered. Press on the **Test List** tab, and select the correct frequency and CL settings for your module.
3. In the **Test List** page, also add any patterns you want to the list, depending on how extensive you want your test to be. When the editing of the list is completed, press **Exit** icon to get back to the Main Operating Screen.
4. In the Main Operating Screen, make sure that the correct file name of the Test File is displayed on the top of the screen. Also, make sure that the tester is in **Connected** status (displayed at the bottom left corner of the screen). Press the **Start** button on the screen to run the test.
5. Press the **Start** button on the screen to run the test and observe the results on the screen. The modules/ICs/pins that fail the test are going to be highlighted on the picture in red color, and the black text window will list the bad pins.

The above testing procedure was performed the quick start for testing a module. Other ways of creating a device file will be described later. More detailed descriptions of the operating procedure and all functions are given in Chapters 4 and 5.



## Chapter 4

# Main Operating Functions

### 4-1 Launching Software Program

After the TurboCATS™ II - 700 system has been properly set up and powered up (refer to Chapter 2), the software program can be launched by double-clicking on the TCII-700 program icon located on your desktop screen.



Figure 4-1 TurboCATS™ II PC700 Software Program Icon

After launching the system application software, the initialization screen will first be displayed showing the TCII-700 software version number and its release date:



Figure 4-2 TCII-700 Software Initialization Screen

The initialization screen will stay up to several seconds, after which the main screen of the application software will be displayed (see Figure 4-3). The Main Operating Screen lets the user set up a customized memory testing procedure. A detailed description of all system functions would be described in this chapter.

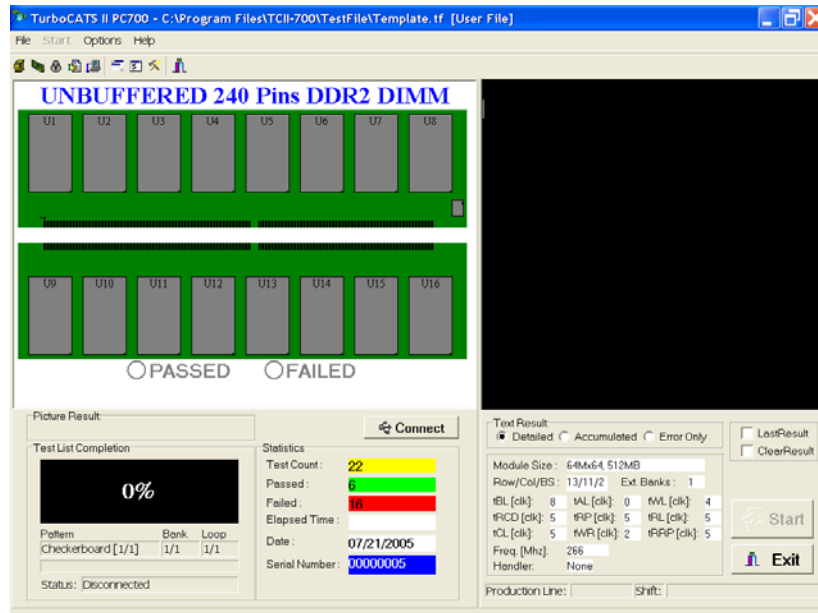


Figure 4-3 TCII-700 Main Operating Screen



**NOTE:** If the software program screens are not displayed properly (don't fit on the PC screen), the user needs to change the PC display setting to a resolution of **1024x768** (under Windows **Start → Settings → Control Panel → Display → Settings**) and font size: **Large Fonts** (under **Display → Settings → Advanced**).

## 4-2 Help Menu

### 4-2-1

### About


The **About** function  will bring up a window with the version # and release date of software you are using.

Figure 4-4  
Help → About Window



## 4-3 Setting Up Test

This section will describe the functions on the Main Operating Screen (shown in *Figure 4-3*) that are used to setup the general system configuration, as well as test procedures for specific types of memory modules.

### 4-3-1 System Configuration


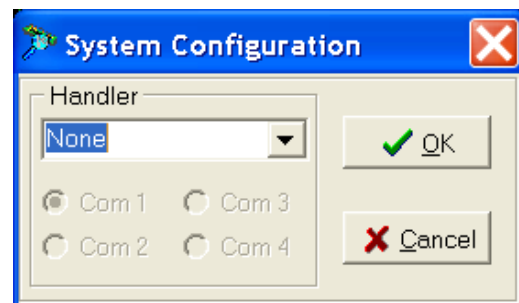
**System Configuration** icon  (this function can also be selected from the **Options** menu on the top of the screen) brings up a System Configuration window on the screen (shown in *Figure 4-5*) and allows the user to setup the **Handler**. It is set to **None** by default. If you are using an Automated Handling System to test your modules, you need to specify its name in this field.

Figure 4-5.  
System Configuration Window



## 4-3-2 Session Information


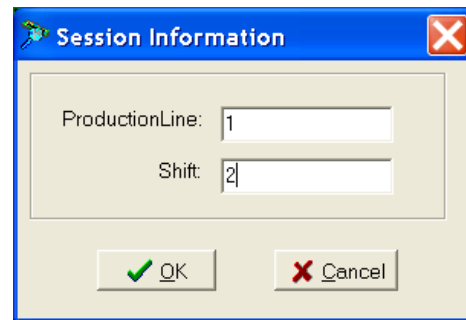

The **Session Information** icon  (this function can also be selected from the **Options** menu on the top of the screen) allows the user to set the **Production Line** and **Shift** numbers to make it more convenient to supervise testing in the production environment. The set numbers will be displayed at the bottom of the screen along with the tester's number. This information will also later be used when creating a test report file.

Figure 4-6.  
Session Information Window



## 4-3-3 Security Privilege

The **Security Privilege** icon  (this function can also be selected from the **File** menu on the top of the screen) allows the user to set the control level of the TurboCATS II-700 system operation. Different users may be assigned one of three security levels: **Operator**, **Engineer** or **Manager** – with **Operator** having the least system access privileges, and **Manager** having the most.

When the software program is opened for the first time after installation, the user takes the security privileges of **Operator** by default. You can click on the **Security Privilege** icon and switch the access level to whatever you want. At this point you can easily go back and forth between the **Operator**, **Engineer** and **Manager** levels of system security. Next time when the TCII-700 software is launched, the system will stay at the privilege level that was set previously when the software program exited. The default privileges (can be changed later) of three levels of access are:

<b>Operator</b>	Can only run the tests, open new Test File, access all functions in the <b>Help</b> menu, and use <b>System Update</b> function (only to open calibration and firmware files, cannot edit/save/upload/download them).
<b>Engineer</b>	Has access to all functions, except the <b>Sorting Table</b> ; cannot upload/download calibration files; cannot reset test count and edit serial number; cannot clear test record database; can access the <b>System Update</b> function (but only to open calibration and firmware files, cannot edit/save/upload/download them).
<b>Manager</b>	Has access to all available system functions, can also change the default list of privileges for each user level, and create / delete users.

You have an option to prohibit certain users from accessing some functions (e.g. if you want some users to only have the privileges of an **Operator** or **Engineer**, and don't want them to be able to change their security level to a higher one). To secure the system access you need to do the

following:

- STEP 1.** Select **Security Privilege** function → **Manager** to access the User Profiles window shown in *Figure 4-7*.
- STEP 2.** On the **Users** page select **Add User** to get the Create New User window as shown in *Figure 4-8*. Enter the user name and password, then select the security level for that user: **Manager** or **Engineer**. Click **OK** to add a new user. You can delete a user from the list later by highlighting his name and pressing **Delete**.
- STEP 3.** On the **Privileges** page select the **Security Level (Operator, Engineer or Manager)**, and optionally add to / delete from the list of corresponding privileges displayed under **Allowed Functions**.

Figure 4-7. Security Privilege → User Profiles Window

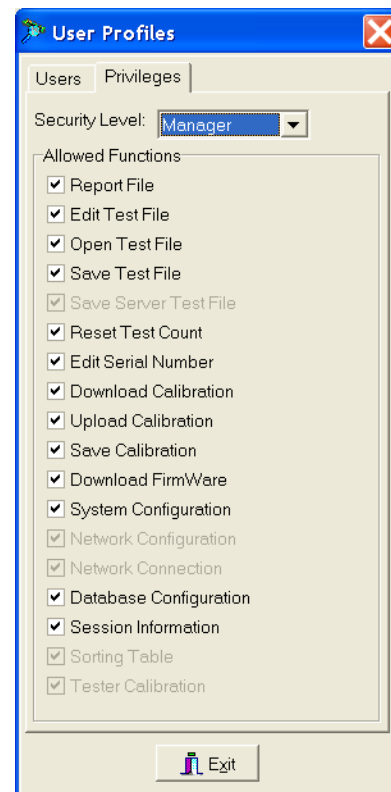
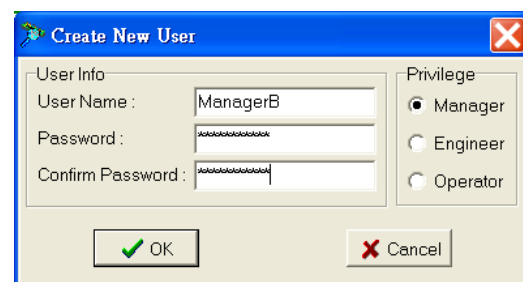


Figure 4-8.  
Security Privilege → Create New User Window



From the moment you add any user profile and exit the User Profiles window the following settings take effect:

- Any user may go to the **Operator** level of system operation at any time. However, whenever the user tries to upgrade the security privilege to either **Engineer** or **Manager**, he will be prompted for the user name and password. Please be reminded that user name and password are case-sensitive.

<b>Operator</b>	Cannot change the security level of system operation to <b>Engineer</b> or <b>Manager</b> without the user name and password.
<b>Engineer</b>	Can change the security level of system operation to <b>Operator</b> at any time, but cannot change it to <b>Manager</b> without the user name and password.
<b>Manager</b>	Can change the security level of system operation to <b>Operator</b> or <b>Engineer</b> at any time.



**NOTE:** These settings take effect even if only 1 user has been defined. The defined user's name and password will be required to upgrade any user's level to a higher one. For example, if only a **Manager** user profile has been created and there is no **Engineers** defined, the user at the **Operator** level would still have to enter the **Manager's** password to get to the level of **Engineer**. Or if there is only an **Engineer**-level user defined, he would still have to re-enter his name and password at the prompt if he wants to access the **Manager** privileges (if no **Manager** has been defined). This prevents an **Operator** from accessing any additional system functions.

- Only users listed on the **Users** page in the **User Profiles** window will be able to log in to access their privileges. Only a **Manager** can add/delete a user.
- **Operator**, **Engineer** and **Manager** users will only have privileges selected under the **Allowed Functions** on the **Privileges** page. All of the same level users have the same privileges. The list of available privileges can be changed, but only by the **Manager** who can access the **User Profiles** window.



**NOTE:** If the **Engineer** forgets his password, then the **Manager** can log in and create a new profile (with a new password) for that **Engineer**. If the **Manager** forgets his password, he needs to contact us for customer support.

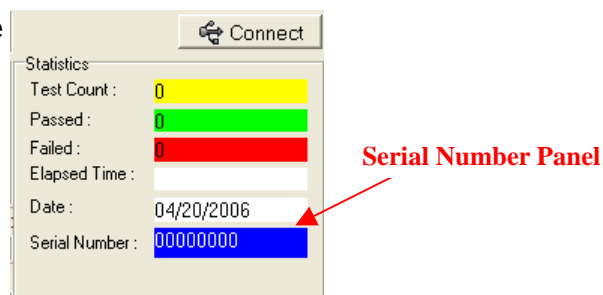
- All user profiles and privileges will be saved when the system is powered down.

## 4-3-4 SPD Serial Number Information

According to Jedec/Intel specifications, for different module, bytes at particular address denote the serial number (S/N) of the module. Triad provides an advanced feature **Serialization** to auto-generate a serial number for SPD write. With serialization on, with the starting initial S/N defined by user, the software will auto-increment the number.

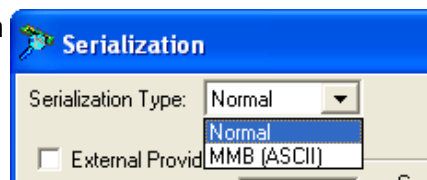
To define the starting S/N, double click on the Serial Number Panel located in the bottom of the main screen which is blue in color as shown in Figure 4-9. This will bring up the serialization page.

Figure 4-9. the Serial Number Panel in the Main Screen



TCII supports normal format and Micro Memory Banking (MMB) format. For different format, select in the combo box on the top (see Figure 4-10).

Figure 4-10. Select Different Serialization Type

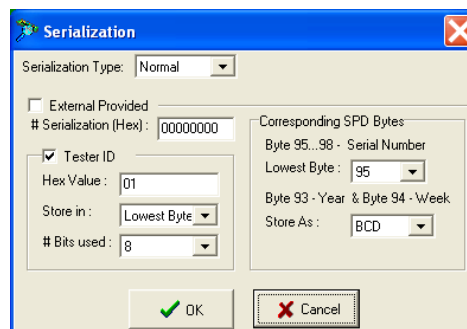


### Normal Mode

The normal mode provide a number of options to configure (see Figure 4-11):

External Provided	Whether user use external source for S/N. With this option checked, the software load the S/N from serial.txt
Tester ID	Whether the S/N includes the tester ID
Hex Value	The Tester ID in hex format
Store In	The Location of the Tester ID in the S/N
# Bits used	Number of bits used to define the tester ID.
Byte 95...98 – Serial Number Lowest Byte:	Defines the address of the lowest byte.
Byte 93 – Year & Byte 94 – Week Store As:	Define the format of year, week: BCD or hex.

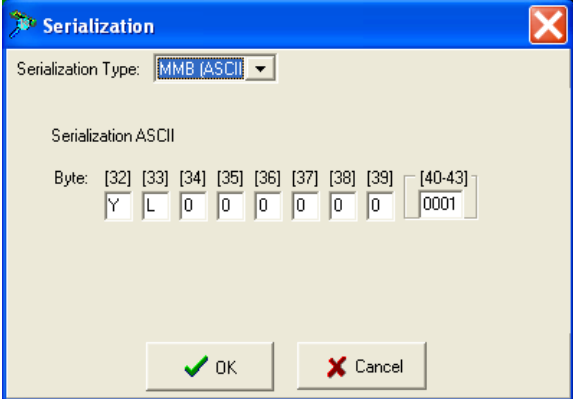
Figure 4-11. Normal Serialization



### **MMB (ASCII) Mode**

For MMB Mode (see Figure 4-12), user defines the S/N in the ASCII character format. Bytes 32-39 are fixed bytes throughout SPD write tests. Byte 40-43 will increase automatically by 1 after each SPD write. Note that as soon as the serial number reaches 9999, user needs to manually modify Byte 39 to make sure the next batch of 9999 modules get a different serial number.

Figure 4-12. MMB Serialization



Serialization

Serialization Type: MMB (ASCII)

Serialization ASCII

Byte: [32] [33] [34] [35] [36] [37] [38] [39] [40-43]

Y L 0 0 0 0 0 0 0001

OK Cancel

Note that each time, the serialization form is open, it will display the current S/N as default

## **4-3-5 Test File**

Prior to running any memory tests on the DUT, the user is required to provide the system with a Test File. The Test File contains all the necessary test setup information, such as DUT configuration: size, speed, etc., and the list of tests to run on it. Testing different modules requires using different Test Files. You need to select an appropriate Test File (open a factory programmed file or create your own) in the Main Operating Screen before you run a test. Below is just a brief summary of how to use a Test File. Chapter 5 will later describe in great detail how to open, edit and save a Test File in order to setup a test procedure for specific types of memory modules.

- The name of the currently selected Test File is displayed on the top title bar of the Main Operating Screen. When the TurboCATS II-700 software program is first opened, the Test File selected for testing is the one that was previously used when the program was closed (or **Template.tf** if the software was just installed).
- To access information in the Test File, you may open it from the Main Operating Screen by either clicking on the **Edit Test File** icon, or going to **File** → **Edit Test File**.
- User can access the Test File through the Test File Editor Screen which contains 3 pages: the **Device** page which contains the information about the parameters of the module, the **SPD page** contains the contents of the SPD EEPROM on the module, and the **Test List** page contains the list of patterns you want to run on your module. You may choose a particular page by simply clicking on its tab on top. All user changes to the Test File are made on these 3 pages, after which you can save your Test File for future use by clicking on the **Save** icon.
- You can change the Test File by clicking on the **Open Test File** icon on top of the screen. It will bring up the **Open Test File** sub-window with the list of all existing Test Files saved in C:\Program Files\Tcii-700\TestFile directory. This list contains several factory-created test files, as well as files that the user created and saved earlier.



- When the Test File is opened and/or edited, the following DUT parameters on the right side of the Main Operating Screen will be updated:

<b>Module Size</b>	module size;
<b>Row/Col/Bs</b>	# of rows / # of columns / # of bank select lines on the module;
<b>Ext. Banks</b>	# of banks on the module;
<b>Operating Freq. [Mhz]</b>	frequency;

Once again, please refer to **Chapter 5** for more information regarding a Test File. Once the Test File is set up, the system is ready to run the tests on your memory module.

## 4-4 Running Test

After the entire test setup is completed (see **Section 4-3**), you can start the actual test by either clicking on the **Start** button on the Main Operating Screen, or by pressing the green **Start** button on the tester.

<b>PC – Tester Connection</b>	The <b>Connect to Test board</b> button allows users to change the connection status of the tester. This status does not take effect during the test setup process (see previous section), but it has to be <b>Connected</b> in order to run the test. When the board is <b>Disconnected</b> , (the tester cannot communicate with it), the DUT cannot be tested and thus the <b>Start</b> button on the screen and the manual <b>Start</b> switch will be disabled.
<b>Start/Stop Button</b>	This button serves as the <b>Start</b> function before and after the test, and during the test it changes to <b>Stop</b> . The user can start the test by either pressing this <b>Start</b> button on the PC screen or by pressing the manual green <b>Start</b> button on the tester. Pressing <b>Stop</b> during the test will stop the test after the currently running pattern is finished.
<b>TestList Completion</b>	This progress bar indicates the percentage of the Test List completed during testing. One Test List is finished when the progressive bar reaches 100% - this means that one loop of all patterns included in the Test List has finished running through all DUT banks. Every new Test List (including the next loop of the same Test List) will reset the progress bar back to 0%.

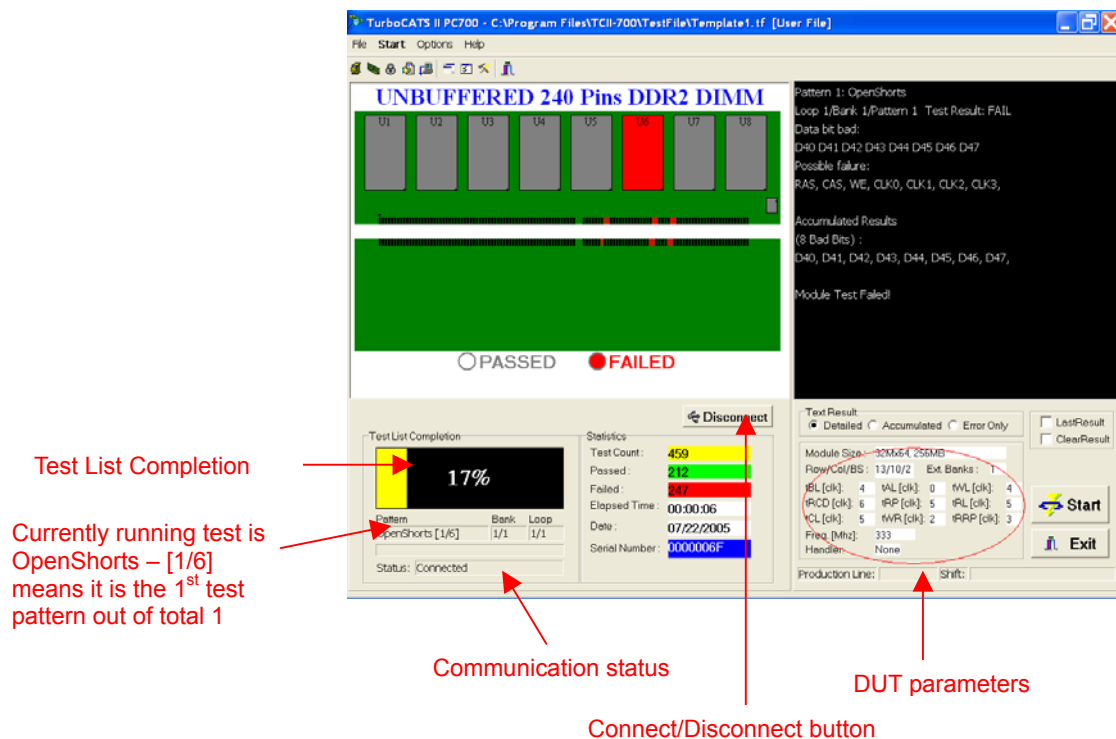


Figure 4-13. Main Operating Window During Test



**NOTE:** On this system, **ONE TEST** is defined as all loops of one Test List (all patterns) completed on all banks of DUT.

Fields in the **Statistics** area on the Main Operating Screen display information useful for production testing:

**Test Count** Total number of tests that have been performed (since the last time the **Test Count** has been reset to 0). Please see the note above for the definition of 'one test'. This value should be equal to the sum of the **Pass Count** and **Fail Count** fields.

**Passed** Total number of tests that passed.

**Failed** Total number of tests that failed.

The values in the above three fields are saved when the software program exits. Therefore, next time when the program runs again, the user can get back to the previous point where he left.

The above fields can also be reset to 0 by double-clicking inside the **Statistics** area (on yellow, green, or red value fields) on the Main Operating Screen. When you do that, a warning pop-up message will give you a chance to cancel this operation. Note that this function will also delete all test records from the database (see Chapter 6 for more information on test records database).

- Elapsed Time** Total time it takes to complete one test on the DUT. See the note above for the definition of 'one test'. The timer will be reset automatically at the beginning of each new test.
- Date** This field displays the current date. If you need to update the date setting on the PC, go to **Start → Settings → Control Panel → Date/Time**.
- Last Result** If this checkbox is checked, the top part of the text result screen will display a picture of the previously tested DUT with its test results.
- Clear Result** If this checkbox is checked, the tester will maintain the communication with the DUT (via reading its SPD) after the test is finished. As soon as the module is removed from the slot, the PASS test results will be cleared from the screen. This prevents the operator from forgetting to press the START button even after the new module is plugged into the slot.

## 4-5 Reading Test Results

Figure 4-14 below illustrates how the TCII-700 software displays the test results. Given below are the detailed descriptions of all available system functions that allow the user to view/study/print out the test results.

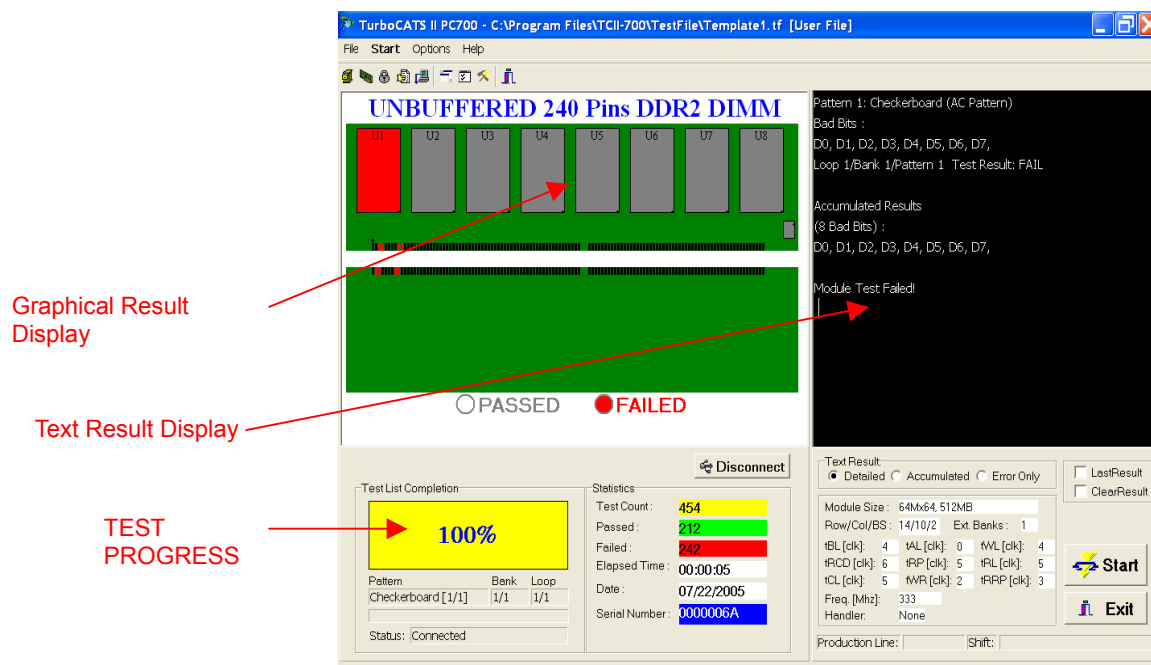


Figure 4-14. MainOperating Window after Test

## 4-5-1 Graphical Result Display

At the end of the test, the appropriate LED under the test board's picture will light up to indicate whether the DUT has passed (green LED) or failed (red LED) the test. The LEDs get reset automatically at the start of each new test.

The TCII-700 system uses the graphical presentation to show the test failures at hardware level (specific ICs, pins, signals that failed):

### Level 1 – Bad ICs

With reference to *Figure 4-14* above, all bad ICs on the module are displayed in red on the Main Operating Screen to make it very easy for the user to pinpoint the cause of the module failure.

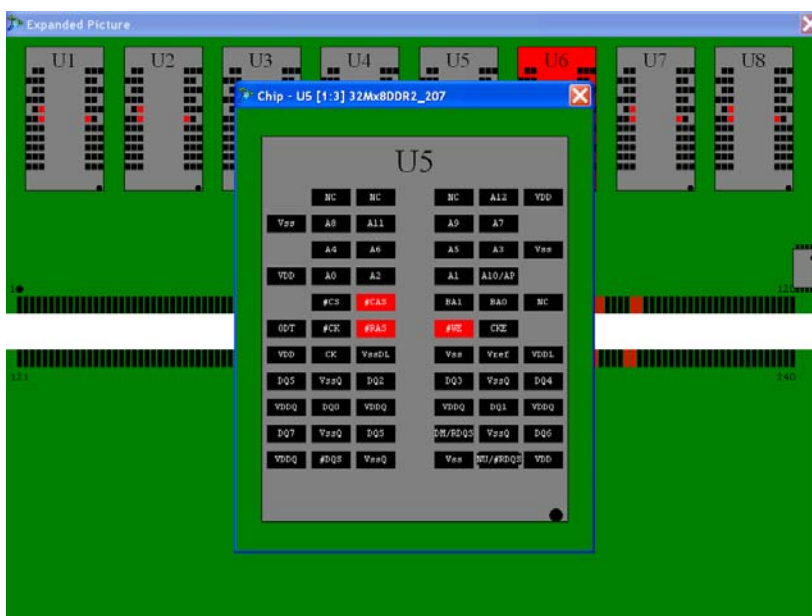
### Level 2 – Bad Pins

To study the graphical display of the module closer, double-click on the picture (anywhere within the picture area). This will bring up a new window with the full display of the board's layout, which clearly indicates the bad module pins and bad IC pins in red (see the background screen in *Figure 4-15*). You can associate the module pins with the IC pins by looking at the pin mapping of the module – right-click on a specific IC on the screen and select **Properties**. This is the same window as the one accessed by clicking on the **Chip** icon on the **Device** page of the Test File Editor window, where the mapping can actually be changed, but the window here is read-only.

### Level 3 – Bad Signals

If you right-click on each individual IC and select **Zoom+**, a new sub-window will show you the actual IC signals corresponding to the bad IC pins in red (see the sub-window in *Figure 4-15* below).

Figure 4-15 Failed Pins & Failed Signals Display



## 4-5-2 Text Result Display

The TCII-700 system uses the black Text Result Display on the right side of the Main Operating Screen to show the test results in the text format. It shows the test failures at two levels: at the hardware level – bad pins are listed, and at the software level – the user can see which test patterns the module failed.

### Changing Display Mode

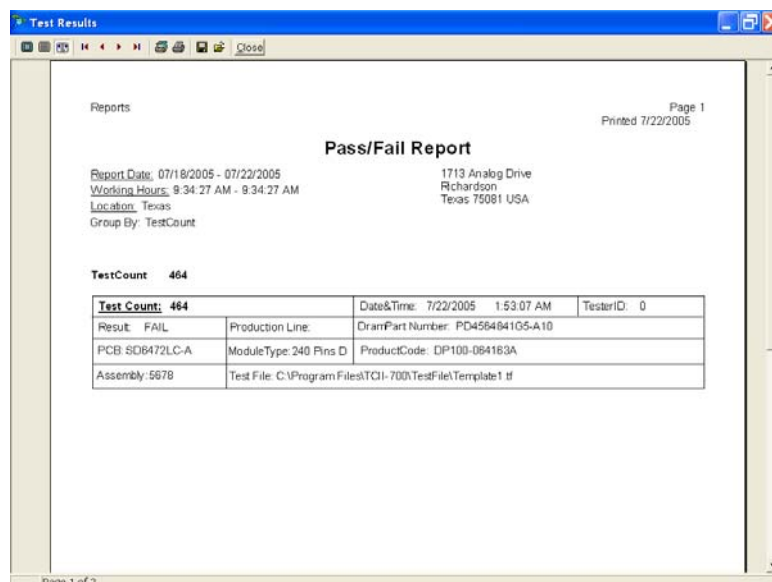
The **Test Result** field under the Text Result Display can be set to **Detailed**, **Accumulated**, or **Error Only** mode. The user may switch between the three display modes at any time during testing.

<b>Error Only</b>	This is the default display mode, in which the screen lists only the failed tests results.
<b>Accumulated</b>	The results of each test pattern will be displayed as <b>Pass</b> or <b>Fail</b> only and the total bad bits accumulated from all test patterns will be displayed in the end for each module bank.
<b>Detailed</b>	The results of each test pattern will be displayed in detail: all bad bits will be listed for each AC pattern, and all the measured values will be displayed for each DC pattern. The accumulated bad bits and results will also be displayed at the end of the test for each module bank.


### Creating Test Report

The TCII-700 software program gives the user an option to create a report with all the test result information observed on the Text Result Display. The test report can then be viewed, saved into a file or printed out. To create a test report, just right-click inside the Text Result Display and select **Preview**. Make sure that you select the desired display mode prior to that: the report can be **Detailed**, **Accumulated**, or **Error Only**. *Figure 4-16* below shows a **Detailed** test report as an example. The function buttons located on top of the screen are described below.

Figure 4-16. Test Report Preview Screen



- Zoom to Fit / Zoom to 100% / Zoom to Page Width**      adjusts the report display
- First Page / Previous Page / Next Page / Last Page**      navigates through the entire report
- Printer Setup**      opens a Printer Setup window which allows the user to select the printer for this job and sets the format of the printed documents.
- Print**      prints the report using the printer selected above. The user may select the same printing function without going into the Preview window – right-click inside the Text Result Display window in the Main Operating Screen and select **Print**. Note that this will use the default printer settings: 1 copy of ALL pages.
- Save Report**      opens a Save As window that allows you to specify the file name and the directory where you want to save this report. The system automatically saves the report in the \*.QRP (Quick Report File) format – it can then be opened and viewed using the **Load Report** function described below.
- Load Report**      allows the user to open a previously saved report file (.QRP) for viewing and/or printing. The Load File window that pops up allows the user to specify the name and the directory of the file to be loaded.
- Close**      exits the Preview Report window, takes the user back to the Main Operating Screen.


 **NOTE:** A report file, which is created following directions given here, will contain only the information seen on the Text Result Display – the user cannot control the report file contents. The TCII-700 software program also provides a more sophisticated function to handle the test results and create report files: it's called a **Report File** function. It allows the user to create a database for holding all test records, and then search that database and create report files containing only specific information selected by the user. The **Report File** function is described in detail in **Chapter 6**.

**NOTE:** After observing results on the screen, you might want to go back to the Test File Editor



window to double-check some parameters that you have set there – in this case please note that the test results (highlighted in red) will disappear if you double-click on the board's picture to access its Test File (the text results will be unaffected).

## 4-6 Closing Software Program

The user may exit the TurboCATS II-700 software program by clicking on the **Exit** icon  in the Main Operating Screen. All current user settings (**Security** Level, **Test Mode**, **Test File**, **Test Count**, etc.) are going to be saved and restored the next time the program is launched. However, you do need to make sure you save the Test Files you modified and report files you created – this information is going to be lost if you don't save it.

## Chapter 5

# Test File

### 5-1 What Is Test File

Before you can use TurboCATS II-700 for testing, you must provide it with the necessary test setup information, such as configuration of the module under test: its size, speed, etc. as well as the list of tests you want to run on it. All this information is stored in the system in the form of a Test File. Testing different modules requires different Test Files. You need to select a desired Test File (open a factory programmed file or create your own) on the Main Operating Screen before you run a test. This chapter describes how to open, edit and save a Test File in order to setup a test procedure for a particular module.

### 5-2 Accessing Test File

Each time when the TurboCATS II-700 software program is opened, the Test File selected for testing is the one that was last used when the program was closed (or Template.tf if the software was just running for the first time after installation). The name of the currently selected Test File is displayed on the top title bar of the Main Operating Screen. To access information in the Test File, you may open it from the Main Operating Screen by either going to **File** → **Edit Test File**, or clicking on the **Edit Test File** icon. This will open a Test File Editor screen shown in *Figure 5-1* (file Template.tf is used as an example).

Test File contains the **Device** page, the **SPD** page, and the **Test List** page. The **Device** page contains the information about the parameters of the module (this page is described in detail in Section 5-5). The **SPD page** contains the contents of the SPD chip on the module (described in Section 5-6). The **Test List** page contains the list of patterns to test the module with (described in Section 5-7). You may choose a particular page by simply clicking on the corresponding tab on the top.



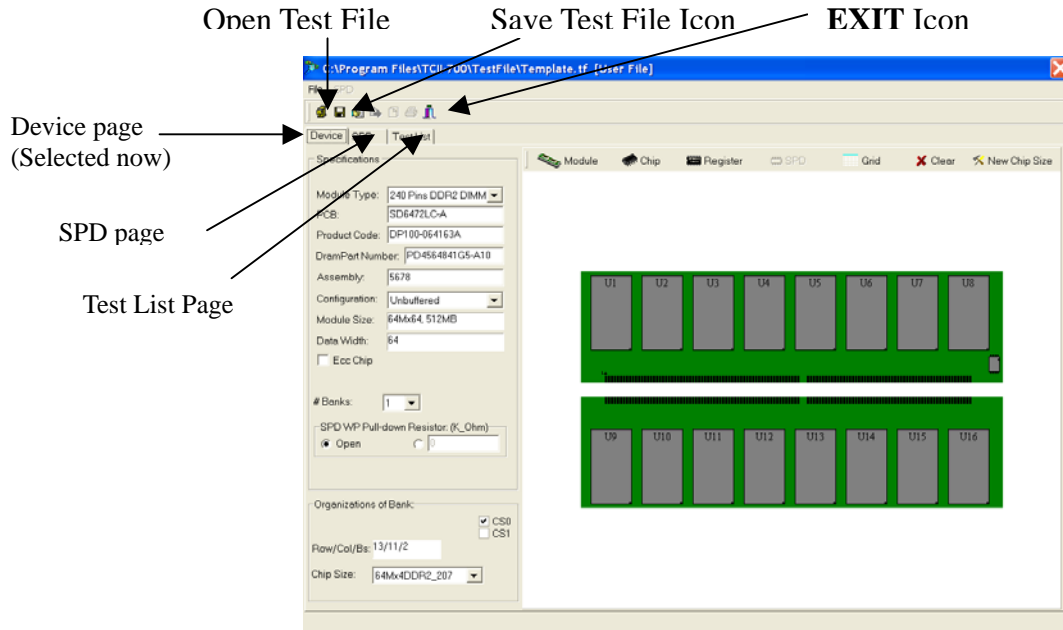


Figure 5-1. Test File Editor Screen

## 5-3 Test File Types

Device page contains the information about the parameters of the module. There are three ways to collect this data, thus two types of Test Files: **User-defined Device** and **Auto ID**. You can select one of these device types for your file in the Save Test File window (see Section 5-8 for instructions on how to save Test File).

### 5-3-1 User-defined Device Test File

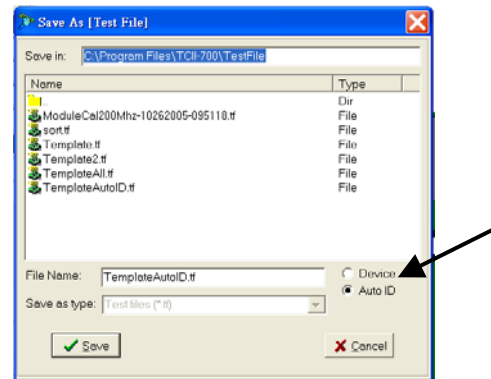
All the parameters set by the user on the **Device** page of the Test File are going to be used to test the module.

### 5-3-2 Auto ID Test File

If Auto ID Test File is used for testing the modules, the system will automatically identify the module parameters before performing the tests selected on the Test List page. It does so by running particular patterns and determining the module parameters from the configuration of the module itself (not its SPD). The parameters displayed on the Device page of the Auto ID Test File before the test are just default values – the correct parameter values are going to be displayed on that screen after the test is finished. The only two parameters you need to set before running the test are the Module Type and Configuration – if these two settings do not match the DUT, then Auto ID function will fail! Refer to Section 5-5-1 for description of two settings.

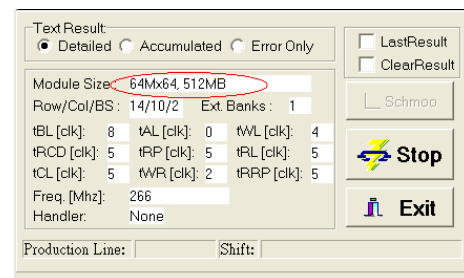
If you want to use Auto ID function, you need to open a Test File with a **.tf** extension. Click on the Open Test File icon and then select to open the **Template.tf** file and choose checked the **Auto ID** (see *Figure 5-2*).

Figure 5-2 Open Auto ID Window



After set up **Auto ID** File, exit to the Main Operating Screen and press the **START** button to start the test. The correct Module Size will be displayed when finished the test (see *Figure 5-3*).

Figure 5-3 Auto ID Result

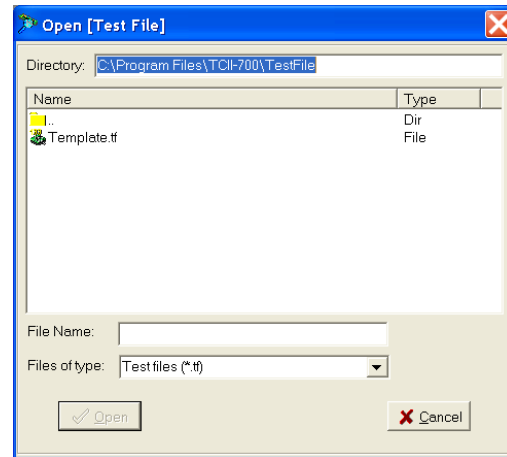


Auto ID function is useful if the user wants to determine the device parameters of a known good module, store them in the Test File, and then use it to test a lot of other similar modules. Note that in this case you must provide a known GOOD module when selecting the Auto ID Test File so that the system can determine the proper parameters.

## 5-4 Opening New Test File

The factory has created a Template device Test File. Click on the **Open Test File** icon on top of the screen to bring up the **Open Test File** sub-window (shown in *Figure 5-4*) with the list of all existing Test Files saved in C:\Program Files\TCii-700\TestFile directory. See *Table 5-1* for description of all Test Files available in that list. The user can open the desired Test File by either double-clicking on its name in the **Open Test File** window or by highlighting its name and clicking on **Open**.

Figure 5-4. Open Test File Window



The user can edit the factory-provided Test File, which includes the desired test patterns and the correct device parameters for the specific module under test. The modified Test File can be saved and used later for testing other similar modules. If the factory-created Test Files are modified, they have to be saved under a different name – the software will not let you to replace existing files. The sections below will explain how to modify and save the Test File.

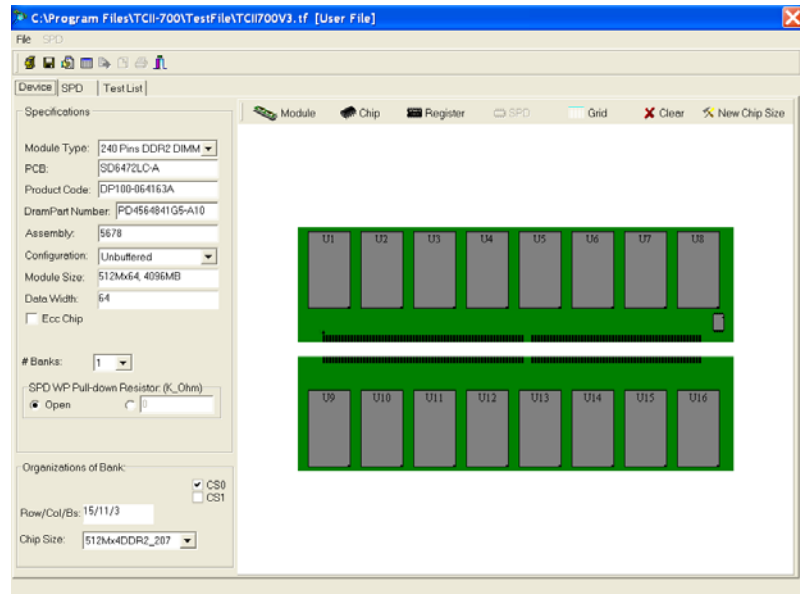
Test File Name	Default Test File Parameters (should be modified for DUT)
Template.tf	Default Module Type: 240-pin DDR DIMM Default Module Size: 64M x 8, 64MB, 1 bank Default Frequency: 266MHz (533MHz data rate) Default Test Patterns: Open/Shorts

Table 5-1. Factory Provided Test Files

## 5-5 Device Editor Page

The **Device** page contains the information about the parameters of the device under test (DUT). You have to provide the test system with the correct DUT configuration in order to achieve valid test results.

Figure 5-5. Device Editor Screen



## 5-5-1 Setting Device Parameters

### Module Type

The TurboCATS™ II-700 system is currently capable of testing the following types of memory modules:

- 184 Pins DDR1 DIMM
- 200 Pins DDR1 SODIMM
- 240 Pins DDR2 DIMM
- 200 Pins DDR2 SODIMM

### PCB, Product Code, Dram Part Number, Assembly

These fields contain user-defined information for a particular module under test. This ID data will be used in the test results report file for user's convenience.

### Configuration

The TurboCATS™ II - 700 system can be used to test both **Unbuffered** and **Registered** modules. Registered module is the one that has address and control lines of each chip buffered. Unbuffered module is the one that's not registered. When registered module undergoes a test, any problems related to the address lines and control lines would be displayed on the register chip(s) on the graphical layout picture.

<b>Module Size</b>	<p>This read-only field shows the module size in the following form: <u>A x B, C</u>, where A = Size of each chip x Number of banks, B = Number of ICs in one bank x Data width of each IC = Data width, C = same module size multiplied out and given in MB.</p> <p>For example, for DUT with <b>Chip Size: 8Mx8</b>, <b># Banks: 2</b>, and 8 chips on each bank (<b>Data Width: 64</b>) – the module size will be displayed as <u>16M x 64, 128MB</u>.</p> <p>If a module has more than 8 chips on either bank, then ‘<b>–ECC</b>’ is automatically added in the <b>Module Size</b> display, showing that the module has ECC (Error Correction Code, a data integrity checking method) implemented on it.</p>
<b>Data Width</b>	<p>This read-only field shows the total width of the module in bits calculated as: Number of ICs on the module x Width of each chip.</p>
<b>Ecc Chip</b>	<p>When this box is checked, the system automatically changes <b>Data Width</b> to 72 bits and places additional ICs in the middle of the graphical layout of the module.</p>
<b># Banks</b>	<p>TurboCATS™ II - 700 testing system is capable of testing memory modules with up to 2 external banks. The number of banks set in this field will automatically be displayed on the graphical layout on the right side of the screen.</p>
<b>Organization of Bank</b>	<p>Use this field to choose the bank for which you want to set the parameters. The number of banks available for selection in the <b>Organization of Bank</b> field depends on how many banks were defined in the <b># Banks</b> setting. The configuration of the selected bank will be displayed in the <b>Row/Col/Bs</b>, <b>Chip Size</b> and Chip Select (<b>CS0</b>, <b>CS1</b>) fields. According to the industry standards, each bank on the device-under-test can have a different configuration.</p>
<b>Row/Col/Bs</b>	<p>This field shows the number of address rows / the number of column address lines / the number of bank select lines (number of internal banks) on each chip used on the module. The information in this field is read-only and depends on the type of chip selected in the <b>Chip Size</b> field.</p>
<b>CS0, CS1</b>	<p>These are two chip select lines. Checked boxes show which CS line(s) are used on a particular bank. If you are testing a module plugged in the front socket, make sure you check <b>CS0</b> or <b>CS1</b> (depending on the bank). With the <b>Dual Module</b> setting, all CS lines are used.</p>
<b>Chip Size</b>	<p>This field displays a list of chip sizes available in the TCII-700 software library. Select the size of the chips being used on the module under test. You can use different IC configurations on different module banks. If you don't see the size you need, you can create a new IC and add it to the library (see ‘<b>New Chip Size</b>’ Icon section below for instructions).</p>

## 5-5-2 Using Device Graphical Layout Icons

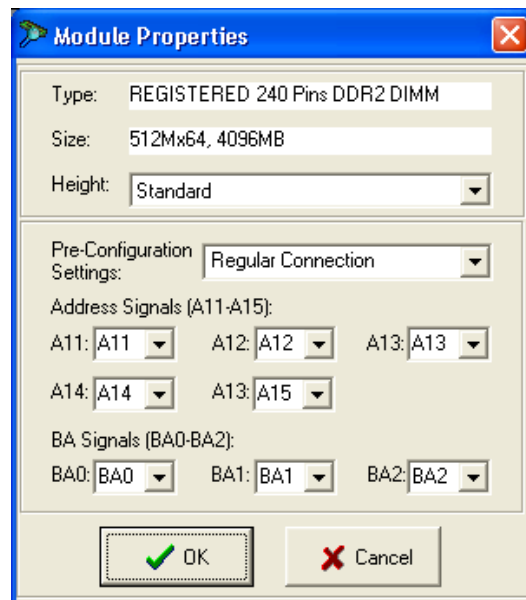
The right side of the **Device** page screen is reserved for the graphical display of the DUT layout. TurboCATS™ II - 700 software shows the picture of the module based on the parameters set by the user on the **Device** page. The user can modify this picture with the help of icons located on the top of the picture screen – the parameters on the left will be changed automatically. There are several icons that the user may use to control the graphical interface when editing the DUT parameters. The functions of each of those icons are described below.

### 'Module' Icon



If the **Module** icon is selected (pressed down), then clicking anywhere on the module picture will bring up the Module Properties sub-window on the screen as shown in *Figure 5-6*. User may then change the **Height** of the graphical DUT display from **Standard** (default) to **Double Rows** to get more space for placing additional ICs on the layout picture (may be needed for x4 modules).

Figure 5-6. Module Properties Window



### 'Chip' Icon


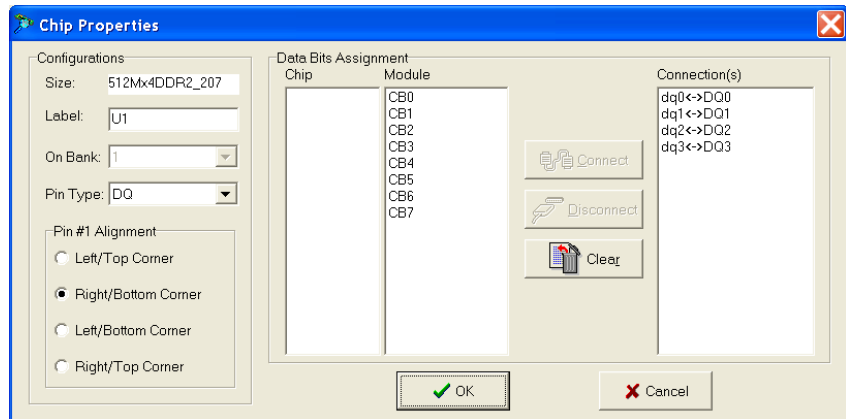
The **Chip** icon  allows the user to add a new IC to either bank on the graphical picture of the module. If the **Chip** icon is selected (pressed down), then clicking anywhere within the module boundaries will bring up the Chip Properties sub-window (shown in *Figure 5-7*), where you can set the configuration of the new IC:

Figure 5-7. Chip Properties Window



<b>Size</b>	IC size is based on the <b>Chip Size</b> field setting on the <b>Device</b> page. If you want to add a chip with size not available in our library, use the <b>New Chip Size</b> icon to create a new chip size (see ' <b>New Chip Size</b> ' <b>Icon</b> section below for more details). Then select it in the <b>Chip Size</b> field;
<b>Label</b>	the default IC label is always set (U1, U2, etc. in order), but the user can change it to any desired name (3 characters max);
<b>On Bank</b>	the bank where the user wants to place the new IC;
<b>Pin Type</b>	select which type of pins you want to map: <b>DQ</b> (data), <b>DQM/DQS</b> , <b>CLKE</b> , or <b>CLK</b> .
<b>Pin #1 Alignment</b>	pin count can be assigned to start in any of the four corners of the IC;
<b>Data Bits Assignment</b>	the user can assign a pin of a selected IC to the particular pin on the module by highlighting both in the <b>Chip</b> and <b>Module</b> columns accordingly, and then pressing <b>Connect</b> . This will place the pin assignment in the <b>Connection</b> column. To delete a particular pin assignment, just highlight it and press <b>Disconnect</b> . To delete all assignments, press <b>Clear</b> . Remember that test results will be displayed according to this pin assignment. The default pin mapping used by the TCII-700 tester is given in <b>Appendix B</b> . Please re-map the pins in this window if the pin assignment given in your DUT specs is different from the tester default.

Press **OK** to place the created chip on the module.

If the newly placed ICs don't fit on the graphical layout of the module, then you need to go to the **Chip Size** field on the left side of the screen and select a bigger size – the picture will automatically adjust to include all the additional ICs.

The Chip Properties window for each IC can later be accessed by right-clicking on that particular chip and selecting **Properties**. The data pin connections can be re-mapped. All of the module data pins available for assignment are listed in the **Module** column – if the module pins have already been assigned, they cannot be assigned to another IC. Each IC can be removed by right-clicking on that particular chip and selecting **Delete**. After an IC is removed, the

associated module pins will be available for assignment to other ICs. The default assignment of IC data pins to the module data pins for DDR modules is given in **Appendix B**.

## 'Register' Icon


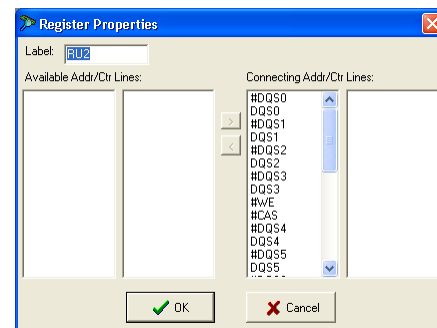


The **Register** icon  allows the user to add the register chip(s) to either side of the module. If the **Register** icon is selected (pressed down), then clicking anywhere within the module boundaries will bring up the Register Properties sub-window (shown in *Figure 5-8*).

Figure 5-8. Register Properties Window




Under **Label** select the name of the register chip you want to add to your module (default names are RU1, RU2, etc.) Two columns on the left under **Available Addr/Ctr Lines** display the list of all available address and control lines (1<sup>st</sup> column) and the list of all ICs on the module (2<sup>nd</sup> column). In the 1<sup>st</sup> column highlight the address or control line you want to buffer through a register chip, then in the 2<sup>nd</sup> column select the IC that line belongs to (multiple ICs can be selected by holding **Ctrl** key), then click on  to place the selected address or control line for a particular IC(s) in the **Connecting Addr/Ctr Lines** columns. When address and/or control lines for particular IC(s) are displayed in the 3<sup>rd</sup> and 4<sup>th</sup> columns, it means they are going to be buffered through your register chip. To remove any of the lines, press . When mapping is completed, press **OK** to place your register chip on the graphical layout picture of the module (*Figure 5-5* has 2 register chips). You may place as many register chips on the module as you want. You can right-click on each of them at any time and choose **Properties** to change the mapping in the Register Properties window, or choose **Delete** to remove the register chip from the module. After a register chip is deleted, all of its mapped lines will become available again for other register chips.


If the DUT was defined as 'Unbuffered' in the **Configuration** setting on the Device page, and the user later places register chips on the module by using the graphical interface, then the **Configuration** setting on the left will be updated automatically to 'Registered'. If the module's **Configuration** is set to 'Registered' from the beginning, the system will automatically place two register chips on the device and map the address lines of all ICs on the module to the RU1 register chip, and the control lines of all the ICs – to the RU2 chip. If a registered chip fails the test, it means that one or more of the control/address lines mapped to it have a problem.




## 'SPD' Icon

SPD icon  is NOT USED in this software version – one SPD chip is already placed on the module by default.

## 'Grid' Icon

Clicking on the icon  will display a grid on the module's graphical layout for easier IC alignment.

## 'Clear' Icon

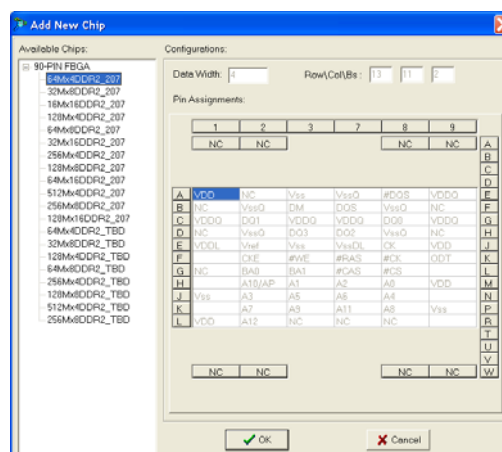
Clicking on the clear icon  will delete all ICs, SPDs and register chips from the graphical picture of the module.

## 'New Chip Size' Icon

If you can't find the right chip-size in the **Chip Size** field on the **Device** page, then you may use the 'New Chip Size' icon  to add a new chip size file to the TurboCATS™ II - 700 tester library following the steps described below. Let's assume we want to add a new file for a chip size 32Mx4 with 13 rows and 10 columns.

- STEP 1.** Click on the **New Chip Size** icon – this will bring up a window with a list of all the available chip sizes as shown in *Figure 5-8*.
- STEP 2.** The chip files in the library cannot be deleted or modified, but they can be copied to create an additional chip size file, which can be modified or deleted if desired. Since parameters of a 32Mx4 chip that we want to add are similar to the ones of the 32Mx4 chip already included in the library (it has 12 rows and 11 columns), we can just copy the existing 32Mx4 chip by highlighting its name, right-clicking on it, and selecting **Create a Copy** (see *Figure 5-8*).
- STEP 3.** Change the name of the new file from "(1) CopyOf32Mx4" to "32Mx4(2)", and then change the **Row/Col/Bs** setting to 13/10/2.
- STEP 4.** Click on **OK** to save the file. Now you can see the new "32Mx4(2)" chip size file in the pull-down menu in the **Chip Size** field and select it for your device. You can always go back and delete the created file by clicking on the **New Chip Size** icon, highlighting the name of your file in the list, right-clicking on it, and selecting **Delete**.

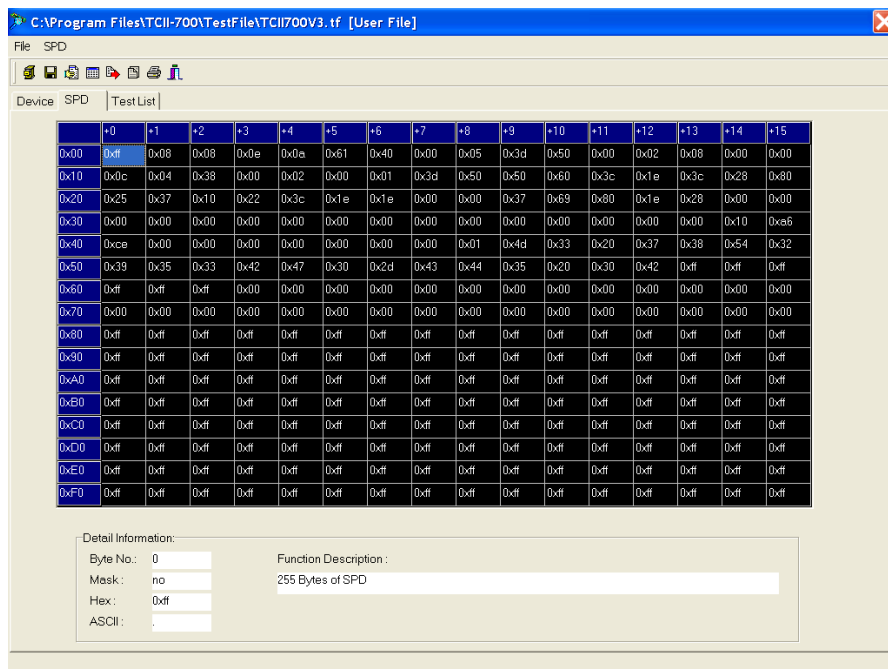
Figure 5-9. Add New Chip Window



## 5-6 SPD Editor Page

The **SPD** page contains the contents of the Serial Presence Detect EEPROM on the module.

Figure 5-10. SPD Editor Page



The file can contain up to 256 bytes of SPD contents. For description of each SPD byte please refer to standard Jedec SPD specifications, but note, however, that certain bytes in the content can be unique to some manufacturers.

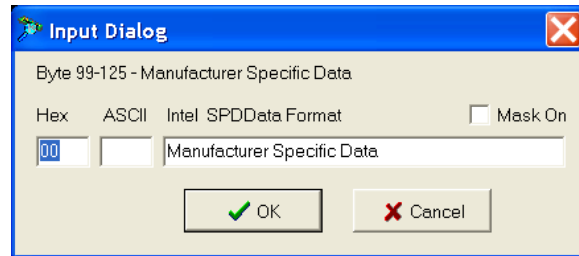
Each Test File can have only one **SPD** page (SPD contents file), since the system assumes by default that each module has only one SPD chip. The **SPD** page of a Test File should contain byte values based on the module parameters set on the **Device** page. If the user runs the **Read SPD** pattern on the module, then after the test is finished, **SPD** page will automatically be updated with the SPD content read from a DUT. An SPD page created and stored by the user in one Test File can be imported and used in any other Test File created for a similar device (see Section 5-6-2 for instructions on how to export and import SPD file). If you are not planning to use the same SPD contents for other Test Files, then you do not need to save an SPD page, only the Test File it's in (see Section 5-8 for instructions on how to save Test File).

### 5-6-1 Edit SPD Contents

On the **SPD** Page, the user can edit each byte of the SPD contents to contain parameters of a specific module type. To modify each value, double-click the byte number to get the **Input Dialog** sub-window for that byte (shown in Figure 5-11).

Note that byte 63 of SPD content cannot be edited. According to the Jedec specifications, byte 63 contains an arithmetic sum of bytes 0 through 62. The TurboCATS™ II – 700 software automatically updates the checksum byte 63 each time the user edits any of the bytes from 0 to 62.

Figure 5-11. SPD Data Input Dialog Window



#### Hex / ASCII

The actual values of SPD content can be entered in either **Hex** or **ASCII** format in these fields. If the value in one field is edited, then the value in another field and the value description in the **Intel SPD Data Format** field are automatically updated.

#### Intel SPD Data Format

This field contains the description of the hex value of each byte based on Jedec DDR SDRAM SPD specifications. The user may edit the description in this field, but it will not update the byte value in the **Hex / ASCII** fields, they also have to be modified by the user. If you want to define any of the empty reserved bytes (128 – 256), you also need to enter the corresponding hex values for those bytes (in that case don't forget to change the number of SPD bytes used for programming/testing under **TestList** → **SPD Program/Test** pattern – the default is 128).

#### Mask On

If this box is checked, the corresponding byte will be masked: it will not be used during the SPD read, program or test. The value of the masked byte is not displayed on the **SPD** page screen.

## 5-6-2 Import SPD Contents

You can import an SPD contents file into your current Test File from another one. To access this function, click on **SPD** at the very top of the **SPD** page to get the pull-down menu, and then


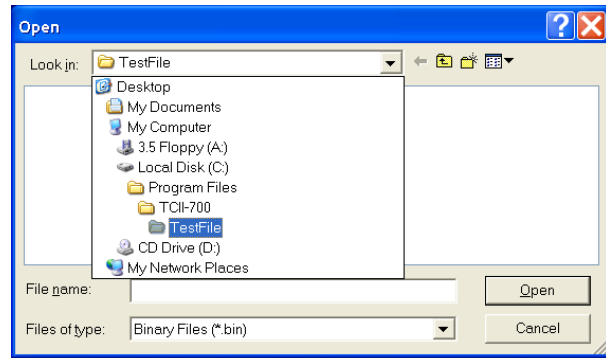

select **Import** . The **Open** window shown in *Figure 5-12* will be displayed containing the list of all available Test Files in **C:\Program Files\Tcii-700\TestFile** directory. You can browse in the '**Look In:**' field and choose your own directory containing the file you want to open. When you highlight the file name and click on **Open**, the SPD page of your current Test File will automatically be updated with the imported SPD data.

Figure 5-12. SPD Import File Window




## 5-6-3 Export SPD Contents


This function allows the user to save the SPD contents from the **SPD** page as a separate file (not a part of a Test File). It can be saved in two types of files: text (\*.txt) or binary (\*.bin). The text file can be later viewed and printed out by using any text editor like MS Word, Notepad, etc., but it cannot be imported back into the Test File. The binary file can be imported to other TCII-700 Test Files.

To access this function, click on **SPD** at the very top of the **SPD** page to get the pull-down menu, and then select **Export** . In the **Save** window, you will then need to select a directory where you want to save your SPD file. You can either select an existing SPD file to overwrite or save your file under a new name. Select the type of file (text or binary) in the '**Save as type:**' field.

## 5-6-4 Create SPD Contents

The **SPD** page of any Test File should contain byte values based on the module parameters set on the **Device** page. If the user changes any parameters on the **Device** page, then this **Create SPD Content** icon  should be pressed to automatically update the SPD data. Note that not all SPD entries will be automatically created. Please double-check each entry after it's been updated by the software – they are created based on the Jedec DDR SPD specs and may not match your particular device. Also note that using Auto ID function to determine device parameters will not automatically create the matching SPD contents.

## 5-6-5 Preview SPD Contents

Click on the **Preview SPD Contents** icon  to bring up a window displaying SPD content in the form of a text file. The data cannot be edited here, only viewed and printed out.

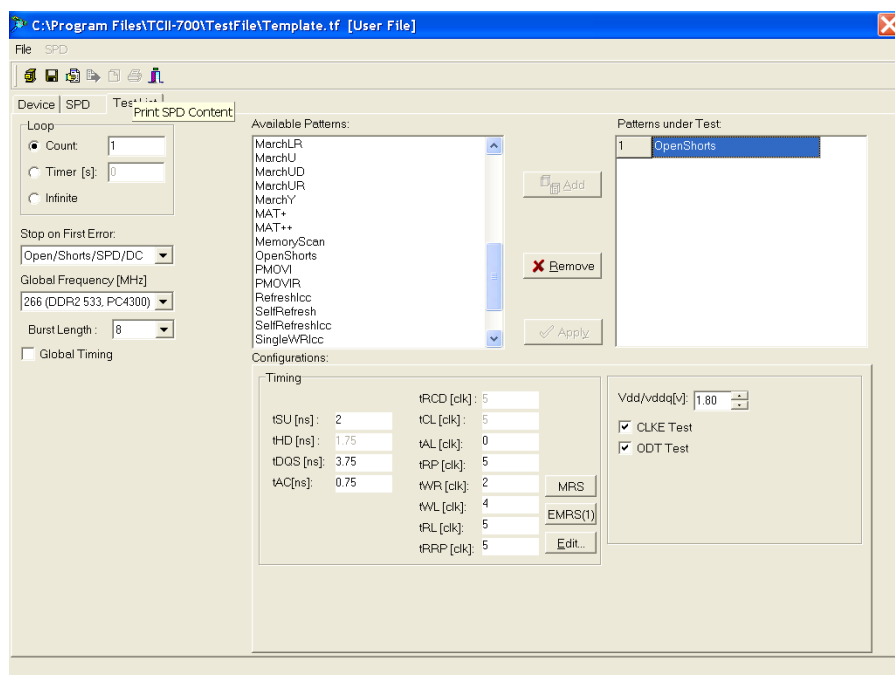
## 5-6-6 Print SPD Contents

Click on the **Print SPD Contents** icon  to print the SPD contents file. You can preview it before printing by clicking on **Preview SPD Contents** icon (see section above).

## 5-7 Test List Editor Page

Through this page, user can select a list of tests that is planned to be run on the memory modules. Note that each Test List should contain at least one test pattern. The factory provides more than 35 memory test patterns to choose from – all of them are listed in the **Available Patterns** column. To place any test pattern in the test list you need to highlight its name in the **Available Patterns** column and click on **Add** to place it in the **Patterns Under Test** column. The user may add several patterns with the same name to the list, provided they are configured with different parameter settings. During the testing process, the tests will be performed in the order they are listed in the column (they will each have a number next to them). If you want to change the order of the test sequence, you can drag any pattern's number field and drop it in the desired location. You may also remove any test from the **Patterns under Test** column by selecting it and then clicking on **Remove**.

Figure 5-13. Test List Page



### 5-7-1 Setting Test List Parameters

#### Loop

The **Loop** function is used to set the number of cycles the user wishes to run the tests for. One loop means that the entire Test List (all included patterns) will run for one cycle. The user may wish to run several loops of the Test List on one memory module to double check its integrity. **Loop** function can be set in three ways:

- Count** – sets the actual number of cycles/loops from 1 (minimum) to 999999 (maximum);
- Timer [s]** – sets the number of seconds from 0 (minimum) to 999999 (maximum) to run loops for;
- Infinite** – will continue looping until the user manually stops the test.

## Stop On First Error

This function makes the system stop immediately if the module fails any of the specified test patterns. This function contributes to the efficiency on the production floor by letting the user know immediately when a module has failed any one test (instead of letting it run through the entire test sequence only to find out later that it failed one of the first test patterns). Table below lists all available settings for the **Stop on First Error** function. It can be disabled by setting it to **Off**.

Function	Description
Off	Even if the module fails one or more of tests, the testing procedure will continue until all the patterns in the Test List have finished running.
Any Test	This setting will stop the test if the DUT fails any of the test patterns.
DC Patterns	This setting will stop the test immediately if the module fails any of the DC patterns: Leakage, or any of the lcc tests. This is useful to prevent damage to the entire memory module in the case where one chip was accidentally misplaced during assembly or rework.
AC Patterns	This setting will stop the test immediately if the module fails any of the AC patterns: AutoRefresh, Checkerboard, DataRetention, HamRd, HamWr, Memory Scan, Self Refresh, Vcc_RW, Volatility, or any of the march tests.
lcc only	This setting will stop the test immediately if the module fails any of the lcc patterns: BurstRWlcc, Refreshlcc, SelfRefreshlcc, SingleWRlcc or StandBylcc.
Leakage Only	This setting will stop the test if the module fails the Leakage pattern.
Open/Shorts Only	This setting will stop the test if the module fails the Open/Shorts pattern.
SPD Only	This setting will stop the test immediately if the module fails the SPD Program/Test pattern, which can include any of the following functions: SPD Program, SPD Test, SPD Write Protect, Slot Test, Serialization, or SPD Read.
Open/Shorts/SPD	This setting will stop the test immediately if the module fails either Open/Shorts or SPD Program/Test.
Open/Shorts/DC	This setting will stop the test immediately if the module fails either Open/Shorts or any of the DC patterns.
Open/Shorts/AC	This setting will stop the test immediately if the module fails either Open/Shorts or any of the AC patterns.
Open/Shorts /SPD/DC	This setting will stop the test immediately if the module fails Open/Shorts, SPD Program/Test or any of the DC patterns. This is a default setting for <b>Stop on First Error</b> function.

Table 5-2. Stop On First Error Function

## Global Frequency [MHz]

This function allows the user to set the operating frequency for the patterns in the selected Test List. For DDR1, the selection frequencies include values from 100 to 220MHz (100, 110, 133, 140, 166, 180MHz, 200MHz, 220MHz). For DDR2, the selection frequencies include values from 200 to 350MHz (200, 220, 266, 280, 333, 350MHz). Note the actual data rate is double the frequency; for example, this field should be set to 200 for PC3200 400MHz modules.

<b>Burst Length</b>	This function allows user to set the burst length to 4 or 8 for Read or Write Operation
<b>Global Timing</b>	For AC patterns, if this box is checked, one set of below timing parameters apply to all test patterns: tRCD, tCL, tAL, tRP, tWR, tWL, tRL and tRRP.
<b>Apply</b>	For AC patterns, apply the selected pattern's tAC, tSU, tHD & tDQS to other patterns.

## 5-7-2 Available Test Patterns

The current TurboCATS™ II - 700 tester supports more than 35 AC/DC parametric test patterns. These patterns are designed to detect and locate various DUT problems, including, but not limited to module assembly problems, open/shorts of SPD EEPROM lines, memory cell leakage problems, device power consumption problems, memory cell stuck-at faults, transition faults, coupling faults, link coupling faults, burst stuck-at faults, etc. **Appendix A** contains descriptions of all available test patterns along with a list of memory faults they detect.

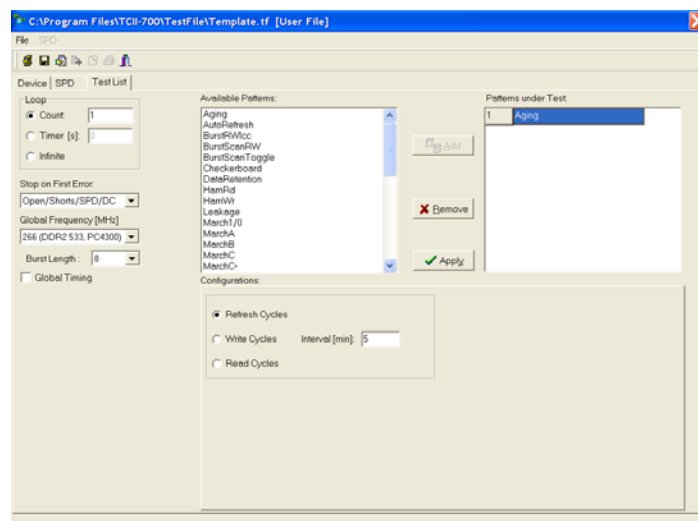
## 5-7-3 Setting Test Pattern Parameters

When a test pattern is selected / highlighted, the screen will change to display the menu of parameters that need to be set for this particular pattern. There are 6 different pattern menu screens overall (some patterns have similar parameters, and therefore, similar screens). Each screen is illustrated below along with the definition of each available parameter. The user can change the parameters of each test pattern either before adding it to the **Patterns Under Test** column or after that. The user may also add the same pattern to the Test List several times, provided that each time it is configured with different parameters.

### Aging Test

Aging test (heating up the module before actual testing) can be performed in one of three ways: by generating continuous **Refresh Cycles**, **Write Cycles** or **Read Cycles** to the DUT. The **Interval [min]** is set to the desired time duration of the Aging test (the value must be in whole minutes), and it defaults to 5 min.

Figure 5-14. Parameter Menu for Aging Test



## Leakage Test

The Leakage test measures the high and low leakage currents on each pin of the DUT while applying high or low voltage accordingly to that pin. This test can be performed on 4 independent groups of **Data Lines, Address Lines, Control Lines** and **SPD Lines**. The user may enable/disable each of the groups, and set the **Low** and **High** voltages applied to them during test. The threshold values of the tested currents are set in the **Currents [uA]** columns based on the DUT specifications. The module fails the test if the measured current values exceed the threshold settings. **Vdd/VddqNom [v]** sets the voltage you want the test to run at.



**NOTE:** If Leakage test fails SPD WP pin, check the value of the SPD WP resistor on the Device page of the Test File.

Figure 5-15.  
Parameter Menu for  
Leakage Test

Leakage Testing		Currents [uA]		
	Low	High	Min	Max
<input checked="" type="checkbox"/> Data Lines	0.00	1.80	-20	20
<input checked="" type="checkbox"/> Address Lines	0.00	1.80	-20	20
<input checked="" type="checkbox"/> Control Lines	0.00	1.80	-20	20
<input checked="" type="checkbox"/> SPD Lines	0.00	1.80	-20	20
Vdd/VddqNom [v]:		1.80	-20	20
CLKE0:	-20	20	-20	20
CLKE1:	-20	20	-20	20
CS [0..1]:	-20	20	-20	20
RAS:	-20	20	-20	20
CAS:	-20	20	-20	20
WE:	-20	20	-20	20
DOM[0..8]:	-20	20	-20	20
DOS [0..8]:	-20	20	-20	20
BS[0..2]:	-20	20	-20	20
A m 151:	-20	20	-20	20

## SPD Program/Test

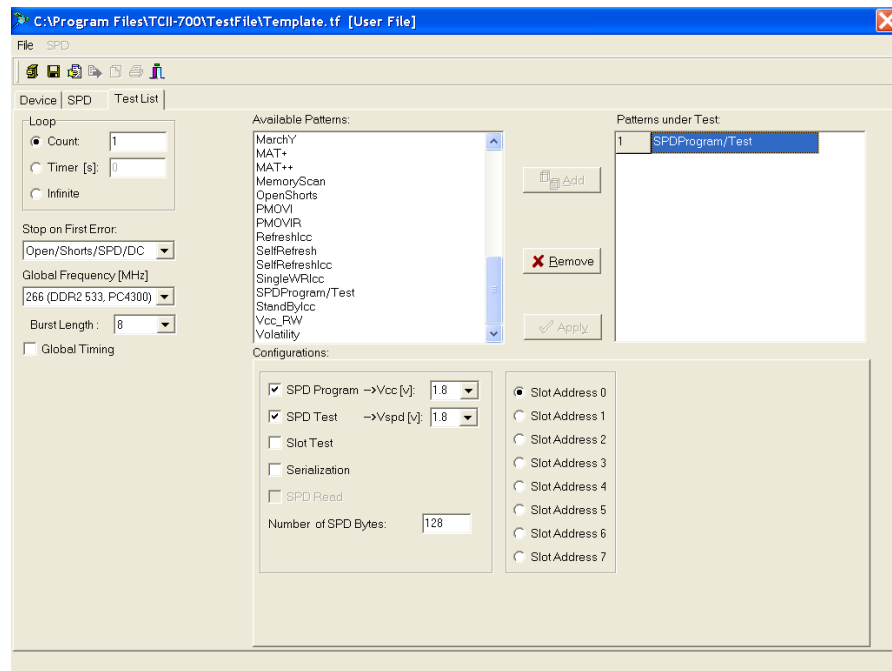
There are several SPD EEPROM test functions under **SPD Program/Test** name: the user can select to program, test or read any selected number of SPD bytes, write protect SPD contents, program SPD with the serial number of the module, as well as test the SPD lines for open/shorts.

### SPD Program

is used to program the SPD of the test module with the data on the SPD page of the selected Test File. If this function is selected, please also set the **Vspd[v]** value to the voltage you want to use during programming SPD (the default is 1.8V for DDR). Also set the **Number of SPD bytes** field to the number of SPD bytes you want to program. **Slot Address 0** is selected by default for programming the SPD, but the user may select any other SPD address location if desired. Make sure to uncheck **SPD Program** if you do not want to change the existing SPD content of the module.



Figure 5-16.  
Parameter Menu  
for SPD  
Program/Test



#### SPD Test

will verify the contents of the SPD by comparing its byte values to the ones set in the SPD page of a selected Test File. The user should also select the desired **Vspd[v]** value, and **Number of SPD bytes** to be tested. Usually, **SPD Test** function is used together with and after the **SPD Program** to verify that it was performed correctly, and the same **Slot Address** setting is used for both functions.

#### Write Protect

can write protect the first 128-bytes of SPD memory on some modules by writing to the SPD write protect register. The last 128-bytes of memory will still be available for the user. Note that the write-protect cannot be reversed!

#### Slot Test

will test for open/shorts of the SPD lines: SA0, SA1, SA2, SCL, SDA, and VddSPD. This function can be enabled only when **SPD Program** is selected. Slot Test will program (write to) and then test (read from) all 8 SPD locations: **Slot Address 0** through **Slot Address 7** (addressed by 3 SPD address lines) – that is why the **Slot Address** selection on the right is disabled when this function is selected.

#### Serialization

will program bytes 95 through 98 of the SPD with the serial number of the module, and bytes 93-94 with manufacturing year and week respectively. All the information to be programmed is set in the **Serial Number** window accessed by double-clicking inside the **Serial Number** field at the bottom of the Main Operating Screen (see *Figure 5-16*). You can also include the **Tester ID** to be programmed into the SPD as a part of serialization. Please note that the serial number of the module automatically increments by 1 during the test, so if you want to program SPD of a module with a specific serial number, you need to set [the desired value minus 1] in the **Serial Number** window before running the test. Note that serial number on the screen only gets updated (incremented) at the end of the test, but it does get used during the test.

## SPD Read

will read the contents of the SPD of the module under test and store them in the current Test File. The SPD contents can then be viewed on the **SPD** page of that Test File, which can later be used to program SPDs of other modules (see **SPD Program**). **Slot Address 0** is selected by default for this function, but the user may select any other SPD address location if desired. **SPD Read** function is available for selection only if **SPD Program** is not enabled.

## Number of SPD bytes

contains the number of SPD bytes to be affected by the SPD operations selected by the user. To save test time, this field's value defaults to 128 bytes (bytes 0 through 127), since usually only the first 128 bytes of SPD content contain information, and the other bytes are unused. The user, however, can set this field to include any number of bytes.

## Icc Tests

All of the Icc tests measure the operating Icc current while applying the preset the voltage **Vdd/VddqNom [v]** and the continuous refresh/write/read/etc. cycles depending on particular test type. The module fails the test if the measured Icc value is greater than the **Threshold [mA]** setting. The **Threshold [mA]** value is specific for each module type tested by TCII-700 system, therefore, it should always be set based on known good modules (not on datasheet specs). To achieve accurate test results, first run the particular Icc test on one known good module, disregard the PASS/FAIL status of the test and instead, observe the measured Icc value on the text display screen. Then set that value as **Threshold [mA]** for testing other modules of the same size/type – the test results will then be correct.



**NOTE:** Refresh Icc pattern will often fail if the **Threshold [mA]** value is not set as described above based on a known good module.

Figure 5-17.  
Parameter  
Menu for Icc  
Tests

The screenshot shows the 'SPD' tab in the software interface. The window title is 'C:\Program Files\TCII-700\TestFile\Template.tf [User File]'. The interface includes a 'Device' tab, a 'SPD' tab, and a 'Test List' tab. The 'SPD' tab is active, showing various configuration options for Icc tests.

**Loop:**

- ☒ Count: 1
- ☐ Timer [s]: 0
- ☐ Infinite

**Stop on First Error:**

Open/Shorts/SPD/DC

**Global Frequency [MHz]:**

266 (DDR2 533, PC4300)

**Burst Length:**

8

☐ Global Timing

**Available Patterns:**

- MarchY
- MAT+
- MAT++
- MemoryScan
- OpenShorts
- PMOVI
- PMQVIR
- RefreshIcc
- SelfRefresh
- SelfRefreshIcc
- SingleWRIcc
- SPDProgram/Test
- StandByIcc
- Vcc\_RW
- Volatility

**Patterns under Test:**

Pattern	Test
1	BurstRWIcc
2	RefreshIcc
3	SelfRefreshIcc
4	SingleWRIcc
5	StandByIcc

**Configurations:**

Threshold[mA]: 1500

Vdd/VddqNom[V]: 1.80

Time Operating ICC: 0

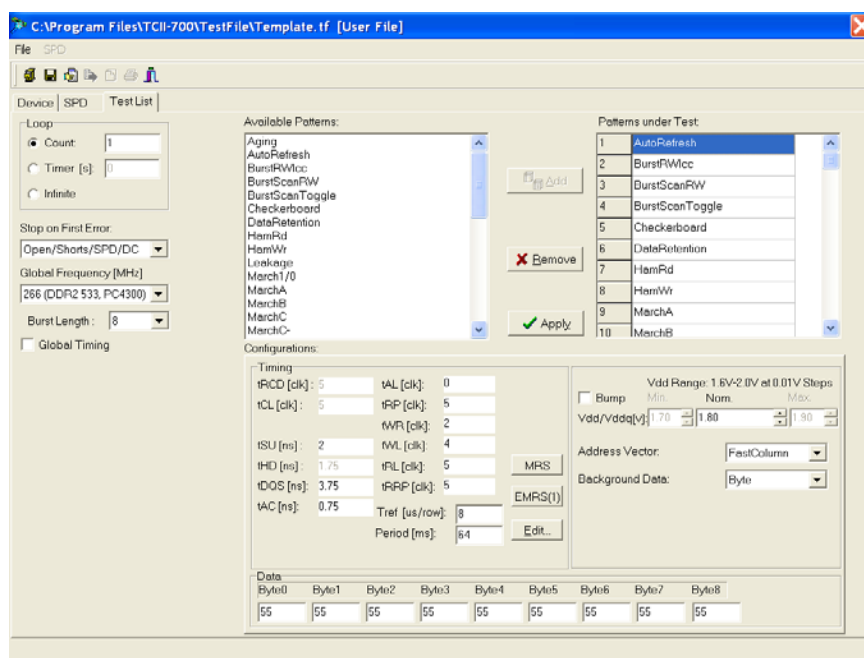
## AC Tests

The following patterns (listed in the alphabetical order) have a similar parameter editor screen: Auto Refresh, Burst Scan RW, Burst Scan Toggle, Checker Board, Data Retention, Ham Rd, Ham WR, March 1/0, March A, March B, March C, March C-, March CR, March G, Marching, March LA, March LR, March U, March UD, March UR, March Y, MAT+, MAT++, Memory Scan, PMOVI, PMOVIR, Self Refresh, Vcc\_RW, and Volatility.

The device parameters described below have to be set before running the test on the module.

- tRCD [clk]** is RAS to CAS Delay (time between Row Access Strobe and Column Access Strobe), written in clock cycles (1 to 8 for DDR2). Press **Edit** to change this parameter.
- tCL [clk]** is Clock low-level width, written in clock cycles (2 to 6 for DDR2). Press **Edit** to change this parameter.
- tSU [ns]** is input (including control, address) setup time. Press **Edit** to change this parameter. When you set this parameter, then **tHD** is automatically calculated as **(CLK – tSU)**. CLK time depends on the frequency of the module set in the **Global Frequency [MHz]** field (for example, for 100MHz module 1clk cycle = 10ns, and for 133MHz 1 clk cycle = 7.5ns).
- tHD [ns]** is the DQ and DM input hold time. Press **Edit** to change this parameter. When you set this parameter, then **tHD** is automatically calculated as **(CLK – tSU)**.
- tDQS [ns]** CK to valid DQS-in. Press **Edit** to change this parameter.

Figure 5-18. Parameter Menu for AC Tests



<b>tAC [ns]</b>	is DQ output access time from CK/CK-. Press <b>Edit</b> to change this parameter.
<b>tRP [ns]</b>	is the pre-charge command period. Press <b>Edit</b> to change this parameter.
<b>tAL [ns]</b>	is the time of additive latency. Press <b>Edit</b> to change this parameter.
<b>tWR [ns]</b>	is write recovery time. Press <b>Edit</b> to change this parameter.
<b>Vdd/Vddq[v] Nom</b>	is the nominal voltage that the selected test pattern is going to run at, but the user can change it to any desired value ranging from 1.6V to 2.0V. For DDR2 modules this parameter defaults to 1.8V with +/- 2% tolerance for each test pattern, but the user can change it to any desired value ranging from 1.6V to 2.0V.
<b>Tref [μs/row]</b>	is the refresh rate, preset by the factory to 8 μs per row. This value is obtained from the device specs as period / number of rows.
<b>Period [ms]</b>	is a refresh period, preset to 64 ms. This is an additional parameter for the AutoRefresh and SelfRefresh tests, which indicates how often will the same row be refreshed.
<b>BurstScanMode</b>	is the burst type ( <b>Interleave</b> or <b>Sequential</b> ). This is an additional parameter for BurstScanRW and BurstScanToggle tests.
<b>Bump</b>	introduces “noise” on Vdd to stress the module under the simulated difficult operating conditions. The supply voltage will fluctuate around <b>Nom.</b> and between <b>Min.</b> and <b>Max.</b> values. For DDR2 modules these parameters are preset to 1.7V and 1.9V respectively, but can be changed by the user to any values between 1.6V and 2.0V.
<b>Address Vector</b>	is a way the address is incremented during the process of writing data to memory. Fast Column will write to one row incrementing the column addresses first, then move on the next row. Fast Row will write to one column first incrementing the row addresses first, then move on to the next column.
<b>Data</b>	contains hex values of bytes <b>Byte0</b> to <b>Byte8</b> that are written to the memory module via 72-bit bus during the test. Values for each byte are pre-set by the factory to either “00” or “55” for each test pattern, but can be changed by the user.
<b>Background Data</b>	is an additional parameter for the few of the tests. The <b>Background Data</b> field sets the pattern of the data that will be written to the module during the entire test. The default setting is Byte, but the user can set it to any of the following:  Byte – Strings of data written to module during test repeat themselves. They are always the same, based on <b>Byte0</b> through <b>Byte8</b> values set in the <b>Data</b> field.  Toggle Byte – After the first 8 bytes of data are written based on values set in the <b>Data</b> field, the next string of data will have <b>Byte0</b> through <b>Byte8</b> inverted. and the data

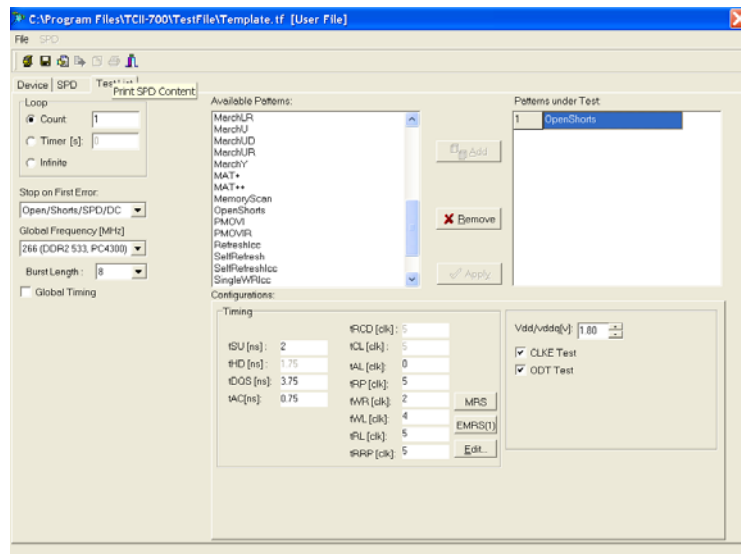
	values written after that will continue toggling.
Col001	– Data bits written are the same as the address of column 0 of the memory (set this way by designer).
Col010	– Data bytes are based on the address of column 1.
Col100	– Data bytes are based on the address of column 2.
Row001	– Data bytes are based on the address of row 0.
Row010	– Data bytes are based on the address of row 1.
Row100	– Data bytes are based on the address of row 2.
RC01	– Data bytes are based on row address XOR column address.
Count	– Every other time each byte is written, it is incremented by one until it reaches maximum value FF, then the value starts back with 0.
Pseudo-Random	– Data is generated by a pseudo-random algorithm.

## Open/Shorts Test

In addition to the timing parameters, which were described above under **AC Tests**, there are several other settings available on this screen:

<b>CS Test</b>	is an option to check Chip Select lines on the module.
<b>DQM Test</b>	is an option to check Data Mask lines on the module (cannot be used with x4 devices!).
<b>CLKE Test</b>	is an option to check Clock Enable lines on the module.
<b>DQS Test</b>	is an option to check Data Strobe lines on the module.

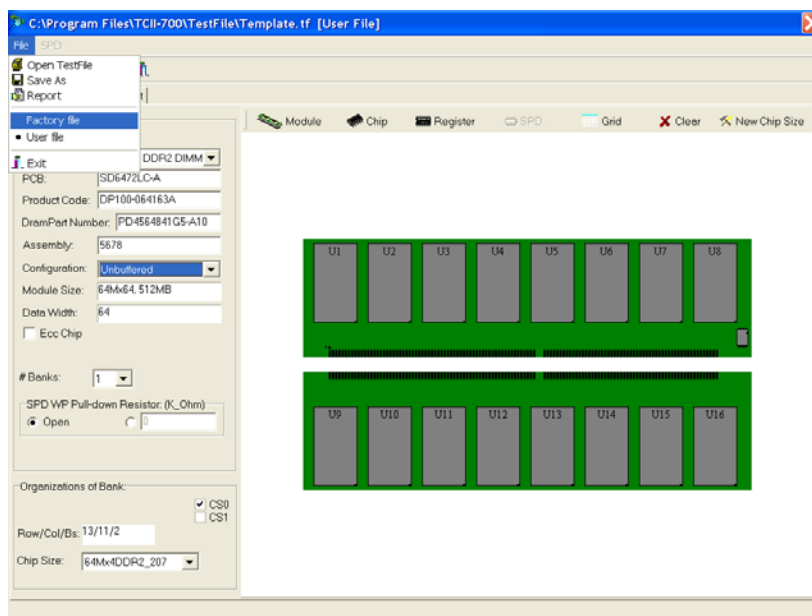
Figure 5-19. Parameter Menu for Open/Shorts Test



## 5-8 Saving Test File

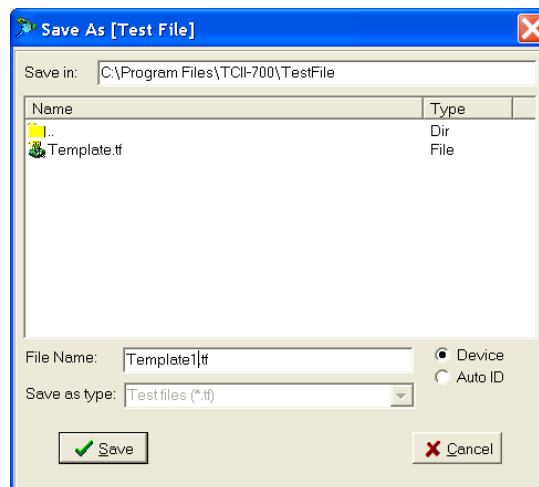
After all the data on the **Device**, **SPD** and **TestList** pages has been edited, the user can save his new Test File. Prior to that, the user should set the security mode for that file. Under the **File** pull-down menu on the Test File screen there are two modes available for selection: **Factory file** and **User file** (see *Figure 5-20*). If the user selects **Factory** file mode, then once the file is saved, he will not be able to edit it, unless he saves it as a different name. If the user selects the **User file** mode (this is a default mode for any Test File), then he will be allowed to modify this file in the future.

Figure 5-20. Setting Test File Security Mode



After setting the mode, click on the **Save** icon on top of the screen to bring up the Save As [Test File] sub-window shown in *Figure 5-21*. Select the **File Name** for your file (either select the existing Test File in the user-file mode to overwrite, or choose a new file name). File extension should be ( **.tf** ). For description of these three file types see Section 5-3. Finally, click on **Save** to save the file.

Figure 5-21 Save Test File Window




## Chapter 6

# Test Result Database

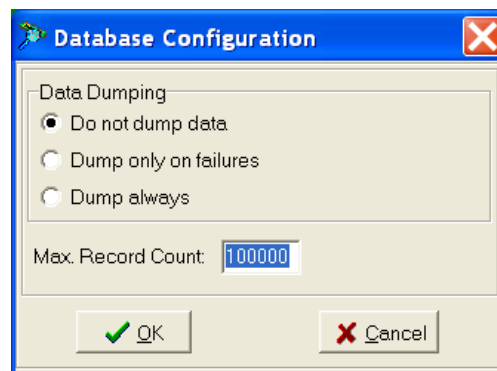
The TurboCATS™ II - 700 software allows you to maintain a database of test records. This chapter will describe how to create and use this database.

### 6-1 Database Configuration

This function is used to create and setup the database for test records. The **Database Configuration** icon  (this function can also be selected from the **Options** menu on top of the screen) brings up a Database Configuration window (shown in *Figure 6-1*) which allows the user to define the **Data Dumping** method (which data should be written to a report log file during the test):

<b>Do not dump data</b>	no log file will be created (default setting);
<b>Dump only on failures</b>	only the failed test pattern information (board #, name of failed pattern, error details, etc.) will be written to the file;
<b>Dump always</b>	the report file will include all the test data;
<b>Max Record Count</b>	defines the limit (6 digits max) of test records to be placed into the system database. The default is 100,000 – one record being defined as all test results from one test run (all loops, all banks) on one module. When <b>Max Record Count</b> is reached, a pop-up message will warn the user that further test runs will overwrite the first records in the database with the new ones.

Figure 6-1. Database Configuration Window



If you select to 'dump data' in the Database Configuration window, then the selected data will be stored in the system database during the test. The database keeps all test results until the user selects to clear it. The current test results are available in the database as soon as the test is finished.

### 6-2 Report File



This function is used to view the entire database of test records, as well as create a report file containing only specific records from the database (by searching the database). The **Report File** icon  (this function can also be selected from the **File** pull-down menu on top of the screen) brings up a Report window (shown in *Figure 6-2*), where all the view/search parameters are set.

Figure 6-2. Report Window

## 6-2-1 View Database

Press the **View Data** icon  to actually view the database of test records. It opens the View Log Data window, which includes two pages (two tabs on top): **Pass/Fail Results** (shown in Figure 6-3) and **Results** (shown in Figure 6-4).

**Pass/Fail Results** You can scroll through the records on the **Pass/Fail Results** page by using the 4 navigator buttons on the top of the screen – **First Record**, **Prior Record**, **Next Record**, and **Last Record** functions. The tabs on top of the record list can be moved to make it easier for the user to group the information he wants to see together. Note that the **Current Test Board** and the **Current Test Count** fields on the top of the screen will change depending on which test record is highlighted/selected.

**Results** When a specific record is highlighted on the **Pass/Fail Results** page – then the **Results** page will contain the details of the test run for that record. If a test pattern is highlighted, the detailed results for that specific pattern would then be displayed on the right-hand side. You can select the format of that display: **Detailed**, **Accumulated** or **Error Only**.

**Clear Database** This function will delete all records from the database and reset the **Test Count** to 0. When you click on this button, a warning pop-up message will give you a chance to cancel this operation.

Another way to clear the database and reset the **Test Count** is to click inside the **Statistics** area (on yellow, green, or red value fields) on the Main Operating Screen. The warning message will appear as well.

**Exit** Returns back to the Report File window.



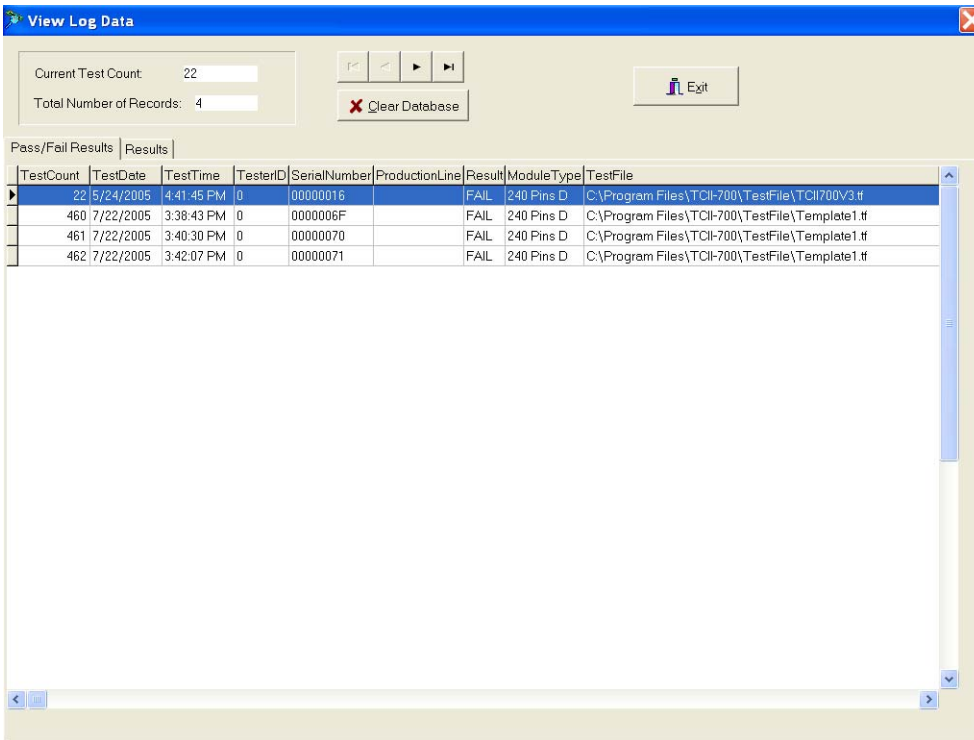


Figure 6-3. View Database Window

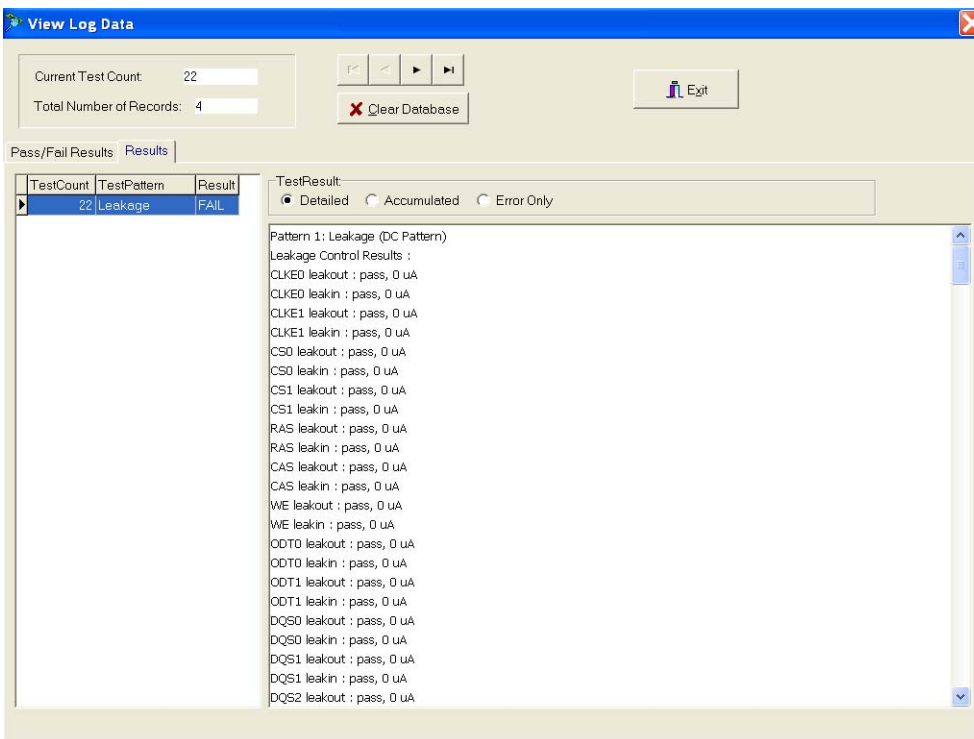


Figure 6-4. View Database Window – Results Page

## 6-2-2 Create Report File

The Report window itself (shown above in *Figure 6-2*) is used to setup the format of the desired report file – the system uses the selections in this window to search the database, find those records that match the criteria, and place them in a report file. The report file can then be viewed, saved, and printed out.

The Report window settings described below allow the user to select which test records from the database are going to be placed into the report file.

**Report Type** can be set to **Pass/Fail Report**, **Accumulated Report**, or **Detailed Report**. **Pass/Fail Report** only has the information about the test result. **Accumulated Report** also includes the accumulated listing of all bad bits at the end of the each test record. **Detailed Report** lists the bad bits for every one of the test patterns in the test list.

**Report Title** allows the user to enter the title for the test report – it would then be displayed on the top of the report. By default the title is set based on the selected **Report Type**: Pass/Fail Report, Accumulated Report or Detailed Report.

**Report From/To** Two pull-down menus allow the user to select the start date and the end date – the results from all the tests performed within that time period are going to be included in the report file. The pull-down menus contain a calendar, which can be scrolled through by using the arrows on top. Select the date by clicking on it. The current date can be easily selected by clicking on **Today** at the bottom of the calendar.

In order to be able to use this function to search the database based on the testing dates, please make sure that the date set on the tester's PC and displayed at the bottom of the Main Operating Screen is correct. If you need to update the date setting on the PC, go to **Start → Settings → Control Panel → Date/Time**.

**Working Hours** The results of all the tests performed within the specified time frame are going to be included in the report file. The hour, minute, second, AM/PM can be adjusted separately by highlighting each and then using the up/down arrows.

In order to be able to use this function to search the database based on the testing times, please make sure that the time displayed at the bottom of the Main Operating Screen is correct. If you need to update the time setting on the PC, go to **Start → Settings → Control Panel → Date/Time**.

**Search by:** provides the user with the option to further limit the number of test records placed in the report file based on the criteria described below. If you do not want to use this option, leave the check box next to it un-checked.

**Test Count** – only test records with the Test Count numbers limited by a certain range will be placed in the report file. You need to specify the range from **Minimum** (0 is not valid) to **Maximum** (up to 6-digits).

**Serial Number** – only test records for modules with Serial Number limited by a certain range will be placed in the report file. You need to specify the range from **Minimum (Hex)** value to **Maximum (Hex)**.

- Result** – only results from the tests that passed will be placed in the report file if **Pass** is selected, and only results from the tests that failed will be placed in the report file if **Fail** is selected.
- Group by:** allows the user to choose an order in which the test result information is going to be placed in the report file.
- Test File** – will group together the result records from the tests that used the same Test File;
- Result** – will first list all the test records with Fail status in ascending **Test Count** order, followed by all the test records with Pass status, also in ascending **Test Count** order;
- Result** – will first list all the test records with Fail status in ascending **Test Count** order, followed by all the test records with Pass status, also in ascending **Test Count** order;
- Test Count** – will list the test record with the smallest Test Count number first;
- Serial Number** – will list the test record for the module with the highest Serial Number first;
- Date Time** – will list the most recent test record last.

The Report File window settings described below only contain the information to be displayed in the beginning of the generated test report for the user's convenience:

- Production Line** is set to PL001 by default, but can be changed by the user. The Production Line number is displayed on the title bar of the Main Operating Screen of the TCII-700 software program itself and can be reset by going to the Session Information window.
- Tester ID** is set by default to the unique ID number given by the factory to every TCII-700 system.
- Location** lists by default the Triad Spectrum, Inc. US factory location, and should be changed to an actual location of the testing site where TCII-700 system is being used.
- Company Address** holds the information about the address of the company using the TCII-700 Memory Test System. The user can choose not to display this information in the beginning of the generated test report by un-checking the box next to this setting.

## 6-2-3 Preview / Print / Save Report File


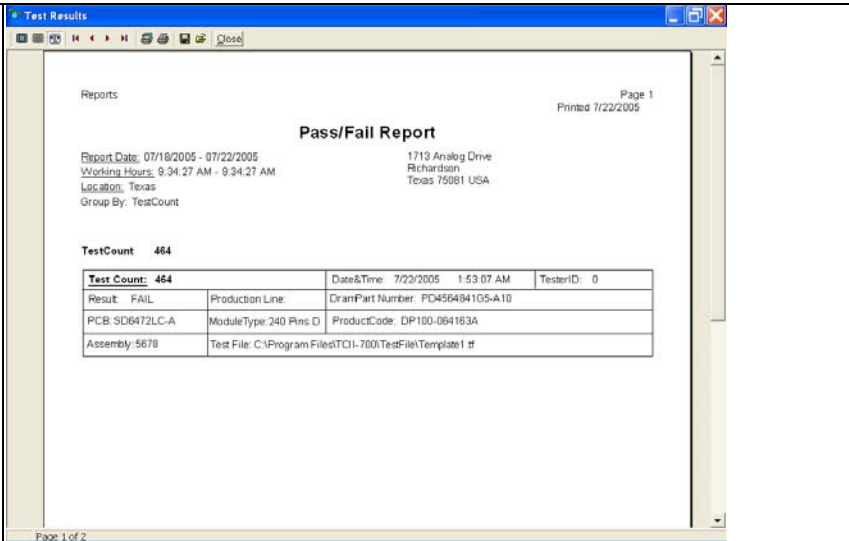
After all the search parameters have been entered in the Report window, press the **Preview** icon  to view the generated report. *Figure 6-5* shows an example of a **Pass/Fail Report** for the specified date and hours.

Figure 6-5. Preview Report Window



The function buttons on top of the screen help you work with the report file:

**Zoom to Fit / Zoom to 100% / Zoom to Page Width**

adjust the report file display


**First Page / Previous Page / Next Page / Last Page**

navigate through the entire report file

**Printer Setup**

opens a Printer Setup window allowing the user to select the printer for this job and set the format of the printed documents. Please make sure that your TCII-700 system is connected to the printer.

**Print**

prints the report using the printer selected above. Note that there is a **Print**  icon in the Report File window itself (next to **Preview** icon), which you can use to print the Report File without even previewing it.

**Save Report**

opens a Save As window that allows you to specify the file name and the directory where you want to save the report file. The system automatically saves the report in a (.QRP) format - it can then be opened and viewed using the **Load Report** function described below.

**Load Report**

allows the user to open a previously saved report (.QRP) file for viewing and/or printing. The Load File window that pops up allows the user to specify the name of the file to be loaded and its directory.

**Close**

exits the Preview Report window, and takes the user back to the Report File window.

## Chapter 7

# Upgrading Software

The TurboCATS™ II - 700 Memory Tester needs to be used with an external PC equipped with Windows 2000 operating system and TurboCATS™ II – 700 software. The latest version of the software available at the time of shipment is included on the attached CD-ROM. Triad Spectrum, Inc. always works to improve the functionality of its products based on the customer feedback, requests and suggestions, and you should check our website frequently for the latest releases of our software. To install the TCII-700 software on your PC or to upgrade the software currently installed on your system, please follow the instructions below. When you use the most current software version available for your TurboCATS™ II - 700 memory tester, it ensures that you get the best possible testing quality and most efficient technical support from us. To see which version of TCII-700 software you are currently using, go to its **Help** menu → **About**.

### 7-1 Downloading Software

All TCII-700 downloads can be found on our website under **Products** → **TurboCATS™ II – 700** → **Downloads**. Make sure you locate the needed software file under the correct tester name and software version! The file (.zip format) for the latest available version will always be on top of the list.

Click on the name of the file to download it (you need to have a Winzip program or equivalent installed on your PC). When you double-click on the name of the file you want to download, it will give you an option of opening it directly from the website or saving it to your local temporary directory first before opening. You will need to come back to that directory and unzip the file after you have downloaded it. Please make sure that you unzip all available software Disks to the same directory. You will need a password to unzip any file (software or firmware) downloaded from our website, so please contact our customer support at [support@triadspectrum.com](mailto:support@triadspectrum.com) for your password. We will need to know your name, the name of your company and the serial number of your tester before we can issue a password. Only customers who have purchased the TurboCATS™ II - 700 tester will be allowed to have access to its downloads. After all files are extracted (unzipped) to a selected directory, it will contain a new folder with several disks.

### 7-2 Installing Software

**STEP 1.** Uninstall the old TCII-700 software version (if applicable):

On your PC desktop go to Start → Settings → Control Panel → Add/Remove Programs → highlight TurboCATS II PC700 → Remove.

An alternative method would be to simply rename your current **C:\Program Files\TCII-700** folder to “\TCII-700 old”, for example, and then install the new software version, which will create a new “\TCII-700” directory. This way you can later rename your old folder back to “\TCII-700” if you want to use it.

**STEP 2.** Install the new TCII-700 software version:

Open the temporary directory where you extracted the zip file → double click on **SETUP.EXE** application file (blue icon) in the **Disk 1** folder and follow the instructions.

It will automatically place TurboCATS™ II - 700 software on your PC under **C:\Program**

**Files\TCII-700** directory. It will also automatically place a shortcut TurboCATS™ II 700 icon on your desktop. Now all you need to do is click on that icon to run the TurboCATS™ II – 700 Software Program.

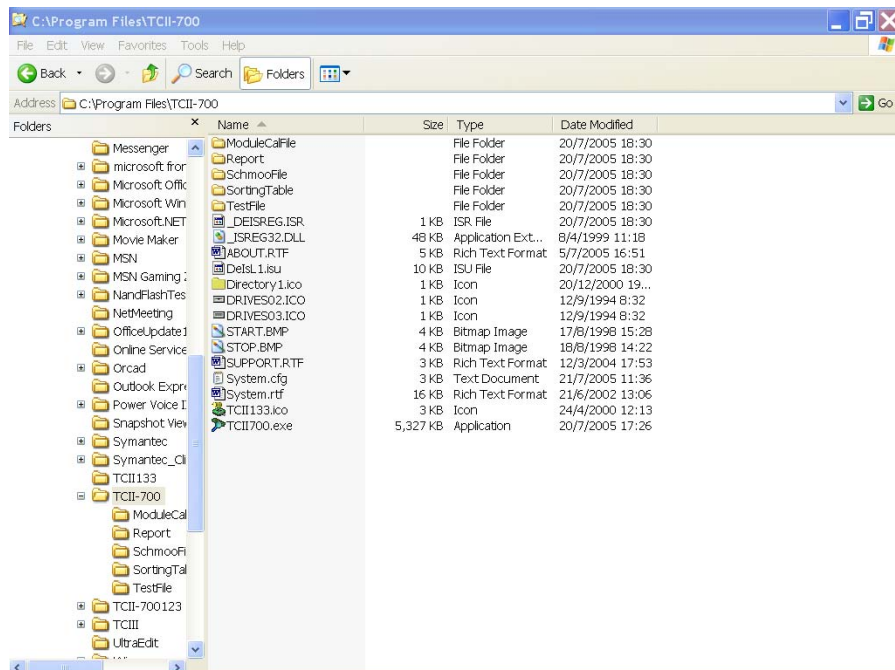
**NOTE:** You don't have to worry about losing all user-created files when you uninstall the current software version and install a new one – the system automatically saves all your test files, calibration, firmware, and report files, and transfers them to the according directories of the new TCII-700 software program. However, to be able to use them with the new software version, the system needs to update the format of those files, and after opening up the new software program for the first time, a pop-up message might ask you whether you want to update your old files. Keep in mind, that if you choose to update all your saved files, they may not be fully backward compatible to the older software versions: you may not be able to use them if for some reason you decide to go back and re-install the old software program. If you think you might ever want to do that, then you need to save all your user-created files in another directory before you un-install the old software program.

Also note that test result database is not saved when the new software version is installed!

**STEP 3.** Install a new driver (if applicable):

Some new software releases may require the system driver to be updated as well – please always check the new software release note. If this is the case, a new driver files **TCIIPC700.sys** and **TCIIPC700.inf** are going to be given on the website as well, and should be placed in the **C:\WINNT\System32\Drivers** directory. Prior to that, the old **TCIIPC700.sys** and **TCIIPC700.inf** files in that directory should be renamed (but not deleted – in case you ever want to go back to the older software version). We recommend that you rename the file to reflect what software version it was last used with, for example, TCII700v10.sys (used with software version 1.0).

Figure 7-1.  
TurboCATS II –  
700 Software  
Directories



## Chapter 8

# Upgrading Firmware and Calibration

### 8-1 Downloading Firmware



Some TCII-700 test system improvements will require not only the new software, but the new firmware as well (logic that gets programmed into the Base board). When this happens, you may be notified by our customer service representative, and the new software release note will mention that the firmware has to be upgraded as well. To obtain the new firmware file, you will need to download it from our website. Please read **Section 7-1 Downloading Software** for general download instructions.



**CAUTION:** If your TCII-700 system needs to be upgraded with both new software and firmware, you need to download the new firmware file to the test board first, and only then install the new TCII-700 software program on your PC (see **Chapter 7**)!

All TCII-700 downloads can be found on our website under **Products → TurboCATS™ II - 700 → Downloads**. Make sure you locate the needed firmware file under the correct tester name and firmware version! The file (.zip format) for the latest available version will always be on top of the list.

### 8-2 Installing Firmware

- STEP 1.** Make sure that both the tester and the PC are powered up and are in working order.
- STEP 2.** Open the temporary directory where you extracted the zip file from the website. Copy the new firmware file (.fw extension) to your **C: \Program Files \TCII-700 \TestFile** directory.
- STEP 3.** Go back to your desktop and double-click on TurboCATS™ II PC700 shortcut icon to start the software program. Select **System Update** function (click on  icon or go to **File → System Update**) to access the **System Update** window → select **Firmware** tab.
- 
- NOTE:** To see which version of firmware is currently installed on Baseboard and its release date, click on **Version Info**. Note that there will be no information provided for the test board if successful communication between PC and tester is not established.
- STEP 4.** Click on **Open File** icon → select the name of the new firmware file you just downloaded from the website → click on **Open**. Now the name of the new file should be in the '**Firmware File Name:**' field in the **System Update** window.
- STEP 5.** When you click on the **Download** icon, the selected firmware file is going to be installed on the test board.

- STEP 6.** Wait until the download process is completed (it takes several minutes). The pop-up message will inform you whether the board has been successfully upgraded. Click on **Version Info** again to make sure that the test board contains the correct new firmware version number.



**NOTE:** If you have downloaded the wrong firmware file to the Baseboard by mistake, simply repeat the above process using the correct file.

- STEP 7.** The tester has to be shut down, and then turned back on for the test board to initialize its new firmware. Close the TCII-700 software program as well, and open it back after the tester has finished the initialization process (the green LEDs next to the manual **Start** switch have stopped blinking). You are now ready to use the test board which is upgraded with the new firmware.

## 8-3 Upgrading Calibration

Our factory has calibrated the Baseboard before your TCII-700 system is shipped. It is recommended that the tester sent back to us for a scheduled yearly calibration to ensure the best testing quality and precise results. Only Triad Spectrum, Inc. has the right to modify the calibration file for each tester. However, you need to have a basic knowledge of how to work with a calibration file in order to be able to upload it from the tester to verify its contents or download it to the tester if we determine it's necessary. This section will cover what you need to know about cal files.

To access calibration files, you need to select **System Update** function inside the TCII-700 software program (the same one that is used for firmware files), and open the **Calibration** page by clicking on its tab on top. The file you observe on the screen is just a template and has all '0' entries.

If you ever have problems with the performance of your test board, we may ask you to view its calibration file to determine whether it got corrupted. To view the cal file currently set on the test board, click on the **Upload** icon (make sure the communication between PC and the tester is established). The cal file contents will be displayed on the screen. If your cal file got corrupted, we will provide you with a backup file.

To upgrade a test board with a new calibration file, perform the following procedure:

- STEP 1.** When you receive any calibration file (backup or custom - .dat extension) from us (we do not place them on the website), place it in the **C:\Program Files\Tcii-700\TestFile** directory.
- STEP 2.** If the TCII-700 software program is currently open, you need to close it and then open it again in order to see the newly added file. Inside the TCII-700 program, select **System Update** function → **Calibration** tab.
- STEP 3.** Click on the **Upload** icon to upload the current calibration file from the Baseboard to the PC. When you see new calibration field values inside the table, save the uploaded cal file by pressing the Save icon. Make sure you give the file the name you can remember – this file is for backup purposes, you may need to download it back to the board later.




- STEP 4.** Click on **Open File** icon → select the name of the new calibration file you just saved in the TestFile directory → click on **Open**. Now the name of the new file should be in the '**Calibration File Name:**' field in the **System Update** window.
- STEP 5.** Make sure that the test board has established communication with the PC software. Click on the **Download** icon to program the test board with a new cal file.
- STEP 6.** Wait until the download process is completed. Use the **Upload** function as described earlier to make sure the selected board contains the correct new cal file data.



**NOTE:** It is not necessary to shut down the tester for new calibration files to take effect. You can obtain the information with the serial # of the test board by uploading the calibration file. We do not recommend our customers to edit/create calibration files themselves (unless under our direct supervision and guidance), that's why we do not provide the description of our cal file entries.

## 8-4 Installing ASIC Code

- STEP 1.** Make sure that both the tester and the PC are powered up and are in working order.
- STEP 2.** Open the temporary directory where you extracted the zip file from the website. Copy the new firmware file (.bin extension) to your **C: \Program Files \TCII-700 \TestFile** directory.
- STEP 3.** Go back to your desktop and double-click on TurboCATS™ II PC700 shortcut icon to start the software program. Select **System Update** function (click on  icon or go to **File → System Update**) to access the **System Update** window → select **ASIC Code** tab.



**NOTE:** To see which version of firmware is currently installed on Baseboard and its release date, click on **Version Info**. Note that there will be no information provided for the test board if successful communication between PC and tester is not established.

- STEP 4.** Click on **Open File** icon → select the name of the new firmware file you just downloaded from the website → click on **Open**. Now the name of the new file should be in the '**ASIC Code File Name:**' field in the **System Update** window.
- STEP 5.** When you click on the **Download** icon, the selected firmware file is going to be installed on the test board.

- STEP 6.** Wait until the download process is completed (it takes several minutes). The pop-up message will inform you whether the board has been successfully upgraded. Click on **Version Info** again to make sure that the test board contains the correct new firmware version number.



**NOTE:** If you have downloaded the wrong ASIC Code files to the Baseboard by mistake, simply repeat the above process using the correct file.

- STEP 7.** You are now ready to use the test board which is upgraded with the new ASIC Code.

# Chapter 9

## Characteristics

### 9-1 Characteristics Feature

Characteristics feature is a new function presented by Triad Spectrum Ltd to provide an automatic mean to discover the characteristics of the system and the device under test. There are totally 3 (*Remark\**) available functions:

- **System Calibration:** realize the optimal calibration parameters for the system.
- **Module Timing:** realize the optimal Test File timing parameters for the system.
- **Schmoo Plot:** realize the passing points in the Test File parameter vector space.

These features are tailor-made for client market need to be easy to use, robust and automatic with little user intervention. This Chapter will describe the function, the configuration and how to run each characteristic function.

*Remark\* There will be one more function known as Bit Mapping released in the foreseeable future.*

### 9-2 Accessing the Characteristics Functions

To access the characteristics page, click on the Characteristic Function Button on the toolbar. The Characteristic Main Page should then open. To access a function, click on the corresponding button in the main page.

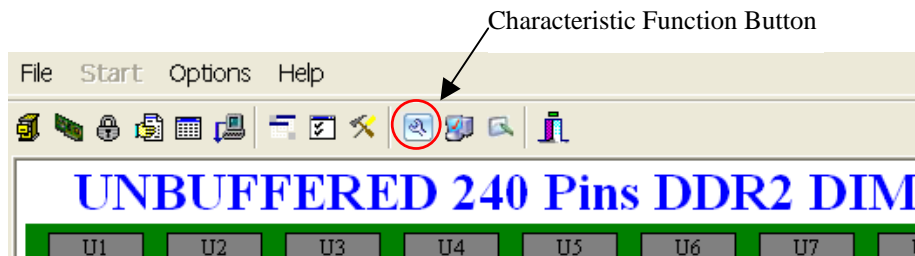


Figure. 9-1 Accessing the System Characteristic Main Page from the toolbar

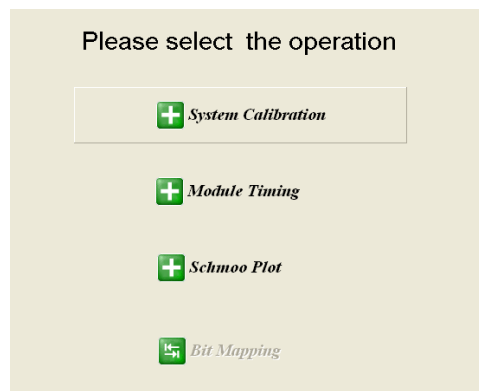
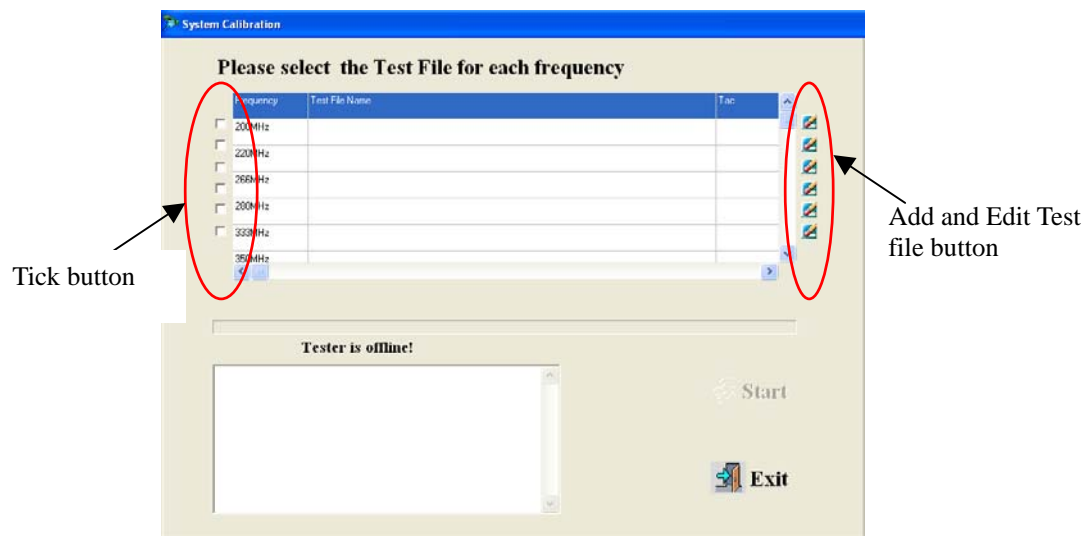


Figure. 9-2 the System Characteristic Main Page

## 9-3 System Calibration

System Calibration realizes the optimal calibration parameters for the system. System calibration works on the following principle: For different frequency, user defines different test files that the system will run tests accordingly. The system will evaluate the optimal calibration parameters according to the test result. The system calibration function page can be accessed by clicking on the System Calibration button in the characteristic main page. This will lead to the system calibration function page (see Figure. 9-3).



**Figure. 9-3 System Calibration Main Page**

Generally, the process of using System Calibration can be summarized into the following steps:

1. Configure System Calibration
2. Run System Calibration
3. Save / Update System Calibration

The following sub-sections will have more detailed description of the steps.

### 9-3-1 Configuring System Calibration

To define the test file for a frequency, user can do either one of the followings:

- i. Click on the "Tick" button (see Figure 9.3) of the frequency to select a pre-defined .tc file.
- ii. Click on the "Add and Edit Test File" button (see Figure 9.3) of the frequency to select a template .tc file. Based on the template file, edit the setting (see Figure. 9.4). Make sure that
  - The module setting is correctly configured.
  - Timing parameters range e.g. Tsu, Tac and Tdqs is correct (To edit the parameters, click on the edit button).
  - The test file frequency correctly matches the selected frequency.Finally exit the page and the software would prompt to save as a new file.

Figure. 9-4 Edit the test file

Frequency

Edit

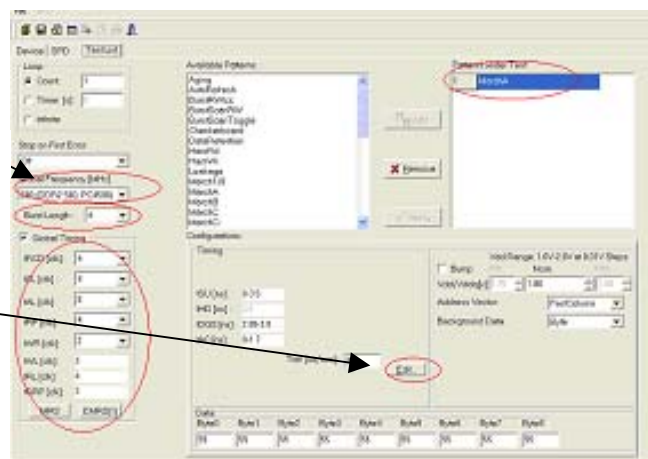
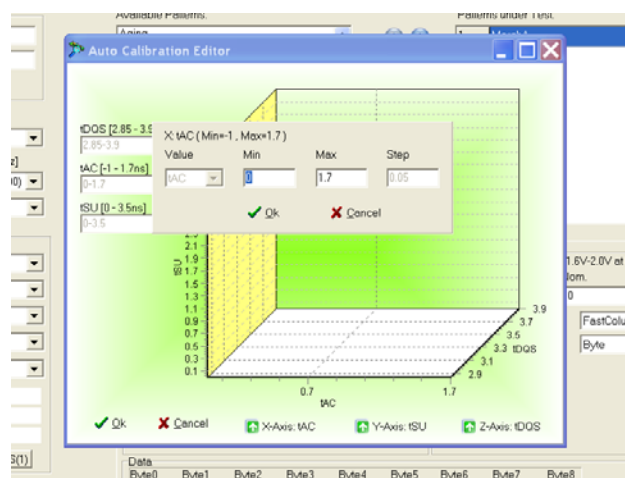


Figure. 9-5 Edit the timing range



## 9-3-2 Running System Calibration

Click on the start button to start the calibration (see Figure 9-6). The result page would be shown. Note that when the calibration completes, the results would be displayed (see Figure 9-6).

Figure. 9-6

Start the calibration

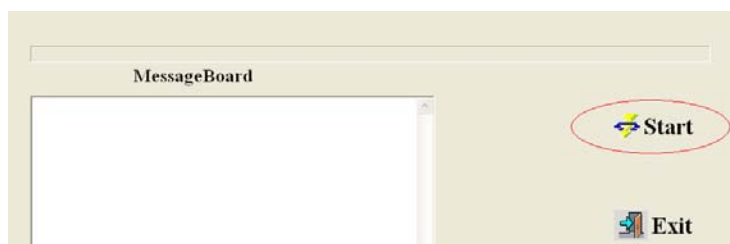


Figure. 9-7

The calibration result

Frequency	Tac Min	Tac Max	Tsu Min	Tsu Max	Tdqs Min	Tdqs Max	Tac Index	Tdqs Index	RecClkSkew	DrvClkSkew	DqsClkSkew
200MHz											
220MHz											
266MHz											
280MHz	0	1.7	0.7	3.25	2.85	3.9	1.6	6.85	3.1	2.7	1.75
333MHz											
350MHz											

Tester Calibration Completed!

### 9-3-3 Saving System Calibration Result

Before saving the result, check the tick button to select the frequency result to be saved. Note that the Calibration file in the tester will not be modified.

Figure. 9-8  
Save the calibration result

Frequency	Tac Min	Tac Max	Tsa Min	Tsa Max	Tdqs Min	Tdqs Max	Tec Index	Tdqs Index	RecClkSkew	DnClkSkew	DqsClkSkew
<input type="checkbox"/> 200MHz											
<input type="checkbox"/> 220MHz											
<input type="checkbox"/> 266MHz											
<input checked="" type="checkbox"/> 280MHz	0	1.7	0.7	3.25	2.85	3.9	1.6	6.85	3.1	2.7	1.75
<input type="checkbox"/> 333MHz											
<input type="checkbox"/> 350MHz											

Tester Calibration Completed!

### 9-3-4 Updating the Calibration File of the Tester

Before updating the calibration file of the tester, check the tick button to select the frequency that the tester calibration would be updated. Click the Update Button to trigger the update. Note that the software would display “Updating Calibration File” during update.

Finally when all the operations are completed, user may click the Exit button to leave the System Calibration Function.

## 9-4 Module Timing

The TCII-700 software provides a Module Calibration Function for automatic detection of the passing range of the DUT. This function is used to find the passing timing range of the modules. The software would also save the middle point of the passing range to a new .mc file that includes date and time. When calibration is performed, the software will test the DUT with multiple loops of the same test pattern until a combination of certain timing parameters is found that passes that module.

Generally, the process of using Module Calibration can be summarized into the following steps:

1. Configure Module Calibration
2. Run Module Calibration
3. Save Module Calibration Result

The following sub-sections will have a detailed description of the steps.

## 9-4-1 Module Timing Configuration

The way to edit the test setting would be identical to that of System Calibration. Please refer to Section 9-3-1 for the procedure.

## 9-4-2 Running Module Timing

Click on the Start button to start the Module Timing. After module timing completes, it will show the summary in the message box. The generated Test File will be shown in the detail page.

Figure. 9-9 Start the test

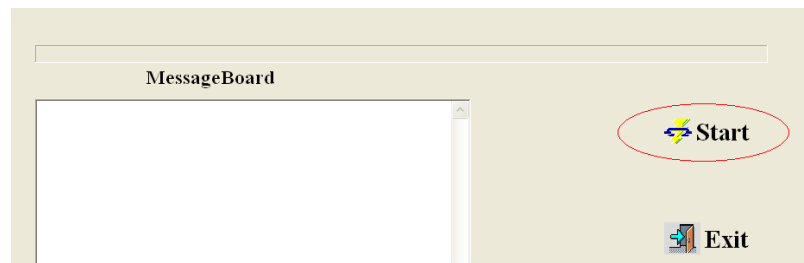
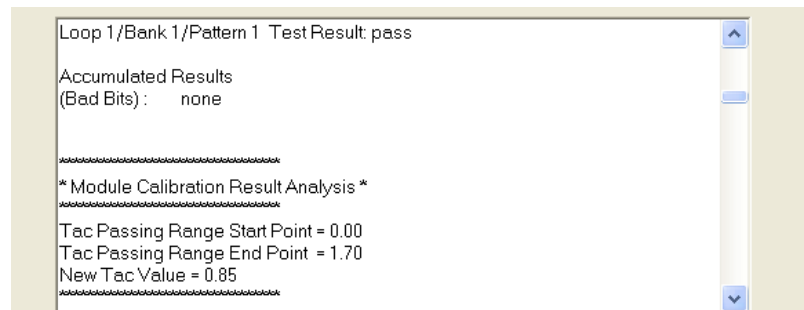


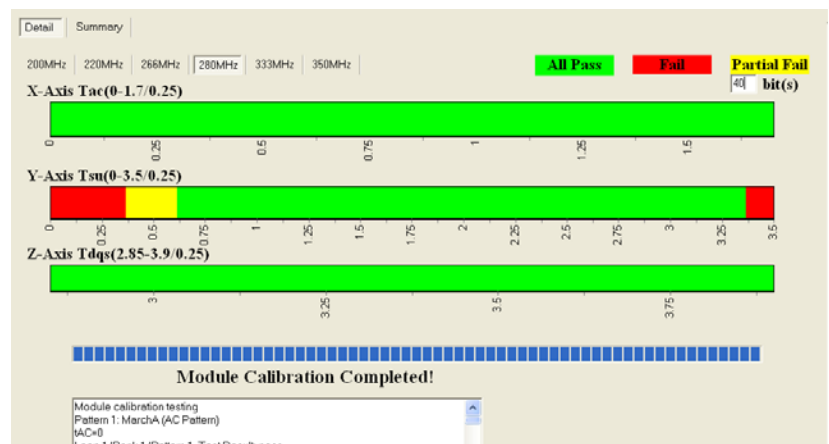
Figure. 9-10 Test Summary



Furthermore, in the detail page, the passing range, fail range and partial fail range will be shown. For Partial Fail box, you can set the threshold fail bits for indication. If the number of fail bits is less than the defined threshold, yellow color will be shown.

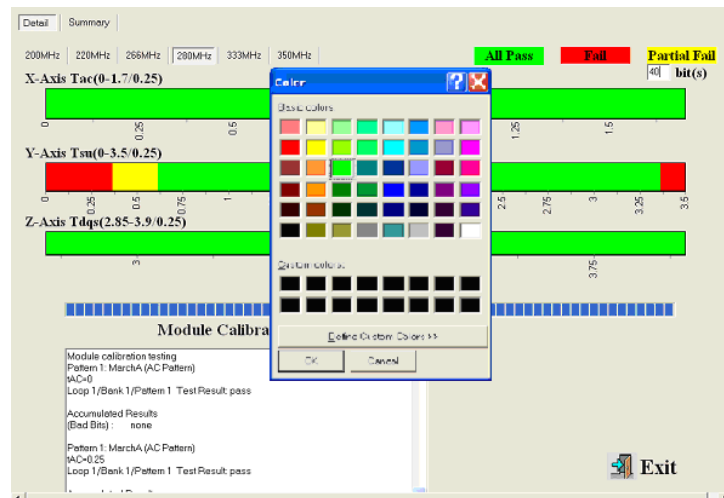
Figure. 9-11

Setting the Partial Fail Threshold



The display color can also be changed by clicking on the All Pass, Fail or Partial Fail panel.

Figure. 9-12  
Changing the Display Color



## 9-5 Schmoos Plot

The TCII-700 software provides the Schmoos Plot function for representing the passing range of the DUT in the graphical format. During this procedure the software will run several tests on the DUT to determine its passing range for the selected parameters, and then plot the test results in either 1-D, 2-D or 3-D coordinates. This is a helpful engineering tool in determining the module characteristics.

### 9-5-1 Schmoos Plot Configuration

To run Schmoos Plot at a frequency, user can do either one of the followings:

- Click on the "Plus" button to select a pre-defined .sp file. (Refer to figure 3)
- Click on the "Add and Edit Test File" button to select a template .sp file (Refer to figure 9-13 to 9-14). Based on the template file, edit the setting (figure 9-15). Make sure that
  - the module setting is correctly configured.
  - Timing parameters range e.g. tSU, tAC and tDQS is correct (To edit the parameters, click on the edit button). (Refer to 9-16)
  - the test file frequency correctly matches the selected frequency.

Finally exit the page and the software would prompt to save as a new file. (Refer to figure 9-17)

Note that for sp file, the dimension of the plot can be varied by selecting different number of parameters (up to three) from tAC, tSU, Vdd, Tref, tDQS (tDQS is for DDR2 only). In other words, the plot can be a 1D, 2D or 3D plot. Please make sure that the dimension is correctly configured.

To remove a .sp test file, click on the "Minus" button.



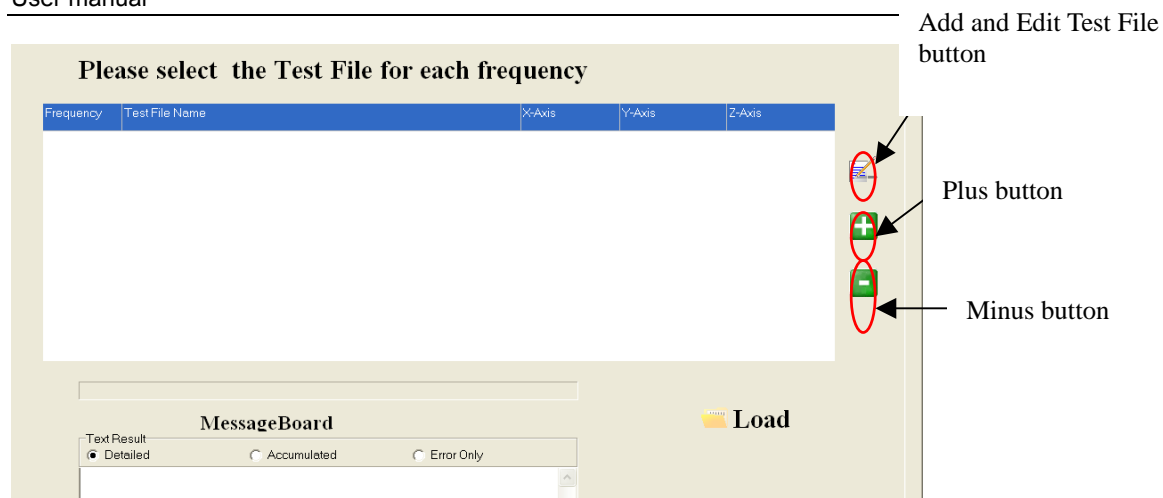


Figure. 9-13 Select the schmoo plot frequency

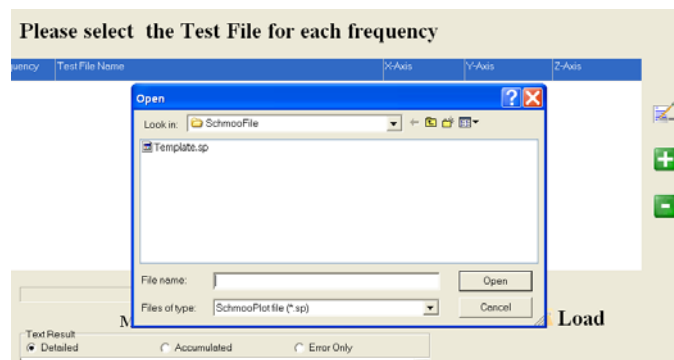


Figure. 9-14 Open the template file.

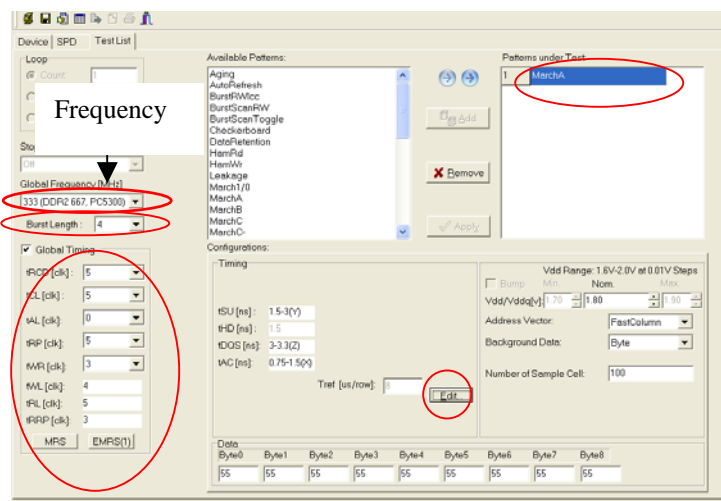


Figure. 9-15 Edit the test file

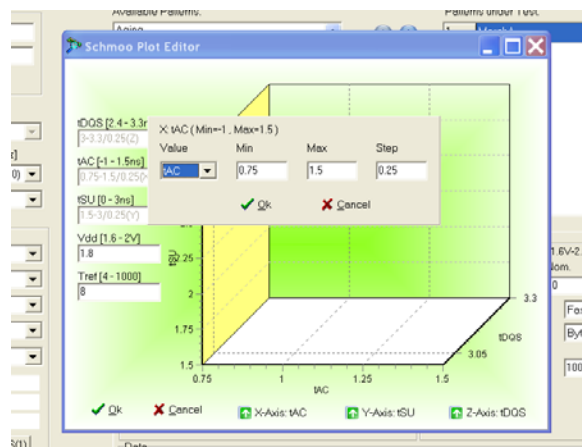


Figure. 9-16 Edit the timing range

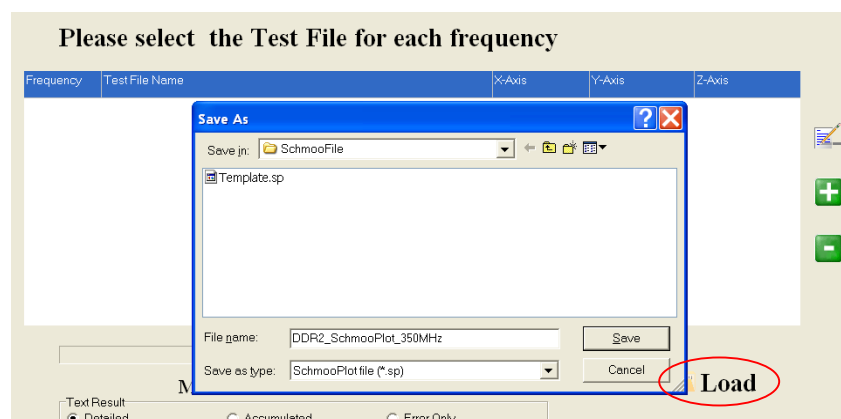


Figure. 9-17 Save the edited Test File.

## 9-5-2 Running Schmo Plot

Click on the Start button to start the plotting. When the plotting completes, the results would be displayed (see Figure 9-18). Also, to enlarge the view picture, click on the Enlarge button on the top view picture.

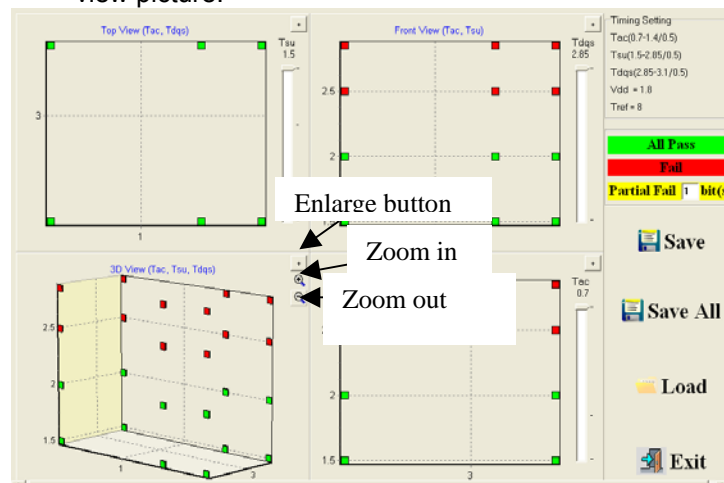


Figure. 9-18 The Schmo plot result

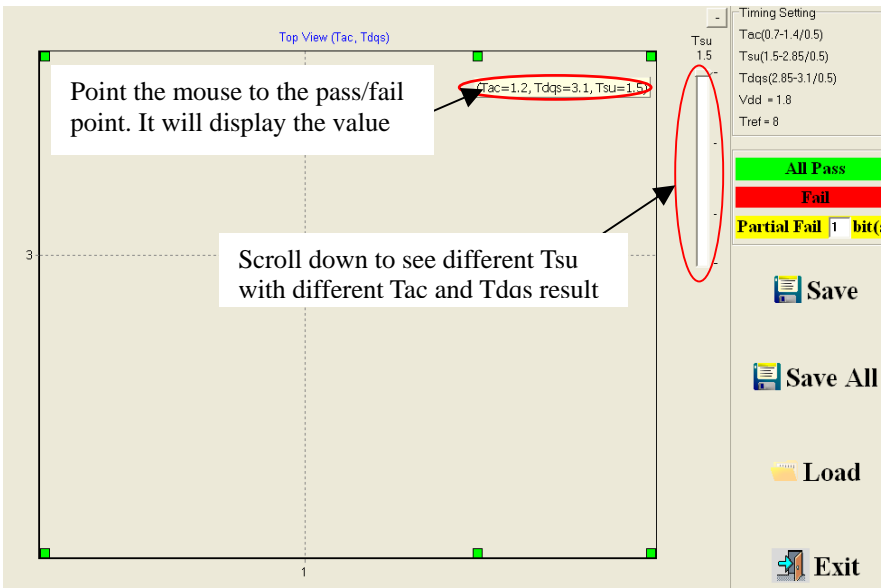


Figure. 9-19 The Schmooplot Top View result

Also note that for each .sp file defined, a plot will be generated correspondingly. In other words, the number of plots will be equal to the number of .sp file selected. To select the desirable plot to view, user can use select the combo box at the top of the window.

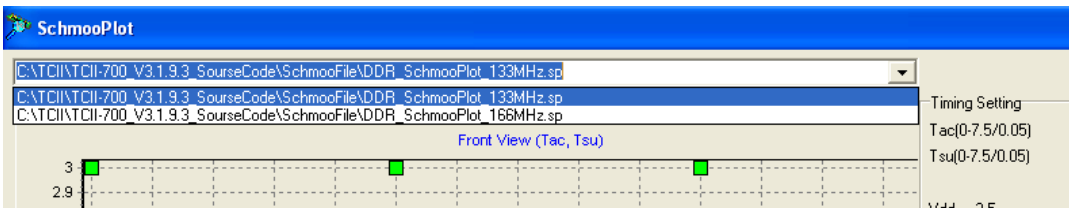


Figure. 9-20 Select the Desirable Plot to View

### 9-5-3 Saving and Loading Schmo Plot Result

User can save the viewing plot result by pressing the Save button. To save all plot result by clicking on the Save All button. To load a result that has been saved in the past, click on the Load button.

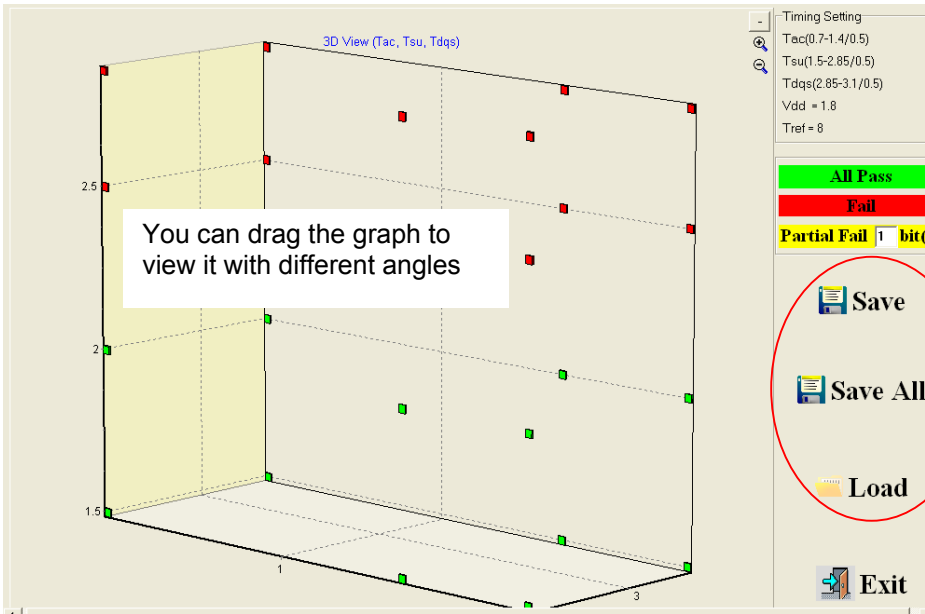


Figure. 9-21 The Schmo plot 3D View result

Click on the Exit button to leave the Schmo Plot function.

## Appendix A

### Test Pattern Definitions

The following abbreviations are used in the table below:

AF – address decoder fault,  
B – number of bits (cells) in the memory word, thus the width of memory  
CF – coupling fault,  
CFdyn – dynamic CF,  
CFid – idempotent CF,  
CFin – inversion CF,  
n – number of bits (cells) in the memory, which equals to  $B \cdot (2^N)$   
N – number of address bits, which makes the number of addresses equal to  $2^N$   
R – read operation,  
SAF – stuck-at fault,  
SCF – state coupling fault,  
TF – transition fault,  
W – write operation.

Test Pattern Name	Test Pattern Description
Aging	The purpose of the Aging test is to detect temperature-related problems in the memory cells by heating up the module first before running the test on it. The Aging time can be set from 0 (min) to 6500 (max) minutes. The system performs continuous refresh cycles, reads or writes (user's choice) on the module for the length of the time interval set by the user.
SPD Program/Test	There are 6 SPD functions available under this pattern name: the user can select to program, test, write-protect or read SPD on the module under test. Serialization function will program certain SPD bytes with the serial number of the DUT and year/week of its production. Slot Test function tests SPD lines (SCL, SDA, VddSPD, SA0, SA1, SA2) for open/shorts.
<b>Electrical Tests:</b>	
Open/Shorts	This test includes the walking address, walking data, and other control line tests that are used to detect shorts in the address lines, data lines, and control lines on the module.
Leakage	The Leakage test measures the high and low leakage currents on each pin of the DUT while applying high/low voltage accordingly to that pin.
BurstRWlcc	This test verifies the operating lcc current in the burst mode.
Refreshlcc	This test verifies the refresh lcc current (in active mode).
SelfRefreshlcc	This test verifies the self-refresh lcc current (test conditions: power-down mode, CKE low).
SingleWRlcc	This test verifies the operating lcc current using the continuous single mode read/write operations
StandBylcc	This test verifies the active standby lcc current in power-down mode (test conditions: CKE low, tcc = $\infty$ ).
Auto Refresh	This test pattern is used to detect the retention faults of the SDRAM during auto-refresh cycle: sleeping sickness fault and refresh line SAF.
Self Refresh	This test pattern is used to detect the retention faults of the SDRAM during

	self-refresh cycle: sleeping sickness fault and refresh line SAF.
Data Retention	This is the test to detect the data retention faults (also called static data loss faults).
Volatility	This pattern tests how well the cells keep data during random voltage fluctuations – voltage is varied after the Write cycles and before the Read cycles.
Vcc_RW	This test is similar to Volatility, but an extra Write is performed to each cell after reading it and before reading another cell – this ensures the precision of Write operations during voltage fluctuations.
<b>March Tests:</b> ( ✓ marks complex patterns)	
Burst Scan RW	It is used to detect all the faults of March A test (see below), plus the burst 4-mode error of the memory. Can be performed in either sequential or interleave burst mode. Example of interleave test pattern: W0,0,0,0 R0,0,0,0 W1,1,1,1 R1,1,1,1...
Burst Scan Toggle	Same as Burst Scan RW, except performed with toggling the alternative bytes, for example: W0,1,0,1 R0,1,0,1 W1,0,1,0 R1,0,1,0
March X	This is a test for unlinked CFins (it also detects AFs, SAFs; and TFs not linked with CFins). It's length is 6*n operations.
MATs+	This Modified Algorithmic Test Sequence + is a short test that detects all unlinked SAFs (it also detects AFs). It allows two or more cells to be read simultaneously, which implies that the used technology does not have to be known. This test takes 5*n operations when use bit-wise and 5*(2^N) operations if used word-wise.
March 1/0 ✓	This is a test for unlinked TFs (it also detects AFs and SAFs). It's length is 14*n operations when use bit-wise and 14*(2^N) operations if used word-wise.
MATs++	This is an optimized Marching 1/0 test with fewer marching elements. It detects all AFs, SAFs, and unlinked TFs as well. This test takes 6*n operations when use bit-wise and 6*(2^N) operations if used word-wise.
March A ✓	This is a test for linked CFids (it also detects AFs, SAFs, TFs not linked with CFids, and certain CFins linked with CFids). It takes 15*n operations.
March B ✓	This is a test for linked CFids. March B is an extension of March A such that it detects, in addition to the faults of March A, TFs linked with CFins or CFids. It takes 17*n operations.
March C	This is the test for unlinked CFins, CFids and CFdyns. It also covers AFs, SAFs, and TFs. It takes 11*n operations.
March C-	This test is an optimized version of March C test (it has one less march element than March C). This is a test for unlinked CFids (it also covers AFs, SAFs, and TFs and CFins not linked with CFids). This test also detects unlinked dynamic coupling faults (CFdyns) and unlinked state coupling faults (SCFs). This test takes 10*n operations.
March CR ✓	Similar to March C, but with read operations performed twice each time in every march element (R-R-W). Takes 15*n operations.
March G ✓	A very complex pattern of 23*n various read and write operations performed in different order, plus extra delays between march elements.

March LA ✓	This pattern consists of multiple (R-W-W-W-R) elements. Takes $22*n$ operations.
March LR ✓	Similar to March U pattern, except the elements are performed in a different order. Takes $14*n$ operations.
March U	This pattern consists of intermediate (R-W) and (R-W-R-W) elements. It takes $13*n$ operations.
March UD	Similar to March U test, but with extra delays added between march elements.
March UR ✓	Similar to March U test, but with extra read operations added to the middle of march elements. Takes $15*n$ operations.
March Y	This is a test that detects linked TFs and CFins, more specifically it detects AFs, SAFs, CFins, and TFs linked with CFins. It takes $8*n$ operations.
PMOVI	Similar to March CR, but with extra read operations performed after write operations, in other words, each march element contains R-W-R. It takes $13*n$ operations.
PMOVIR ✓	Similar to PMOVI test, but with extra read operations added to the end of march elements (R-W-R-R). Takes $17*n$ operations.
<b>Base Cell Tests:</b>	
Checkerboard	This is a simple test to detect shorts between adjacent memory cells, under the condition that address decoder functions correctly. 0's and 1's are written to the memory that's divided into two groups, forming a checkerboard pattern.
Memory Scan	This is a minimal open and shorts test of the memory cells and is similar to the PC memory test pattern performed at boot up. It checks all of the memory cells on the module by writing 0's or 1's and then reading them. This test is also known under a name Zero-One test.
<b>Repetitive Tests:</b>	
Ham Rd	This is a Hammer Read test that performs multiple read operations to a single cell in order to make partial fault effects become full fault effects and detect them.
Ham WR	This is a Hammer Write test that performs multiple write operations to a single cell in order to make partial fault effects become full fault effect and detect them.

## Appendix B

### Default Pin Mapping

The default pin assignment used by all TurboCATS™ software programs for DDR modules is given below. Note that this mapping can be modified for any module by going to **Edit Test File** → **Device** page → **Chip Properties** window (use **Chip** icon).

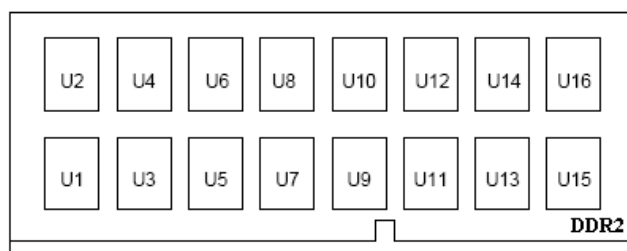
#### B-1 Modules with nMx4 Ics

IC pins	Corresponding module pins
U1: 0 → 3	0, 1, 2, 3
U2: 0 → 3	4, 5, 6, 7
U3: 0 → 3	8, 9, 10, 11
U4: 0 → 3	12, 13, 14, 15
U5: 0 → 3	16, 17, 18, 19
U6: 0 → 3	20, 21, 22, 23
U7: 0 → 3	24, 25, 26, 27
U8: 0 → 3	28, 29, 30, 31
U9: 0 → 3	32, 33, 34, 35
U10: 0 → 3	36, 37, 38, 39
U11: 0 → 3	40, 41, 42, 43
U12: 0 → 3	44, 45, 46, 47
U13: 0 → 3	48, 49, 50, 51
U14: 0 → 3	52, 53, 54, 55
U15: 0 → 3	56, 57, 58, 59
U16: 0 → 3	60, 61, 62, 63

If 'ECC chip' setting is selected, the ECC ICs are automatically added in the middle of the module, and other ICs are shifted accordingly:

U5: 0 → 3	64, 65, 66, 67 (Parity/ECC)
U14: 0 → 3	68, 69, 70, 71 (Parity/ECC)

*Figure B-1.  
Standard 4-Bit IC DIMM Reference  
Designator Map*





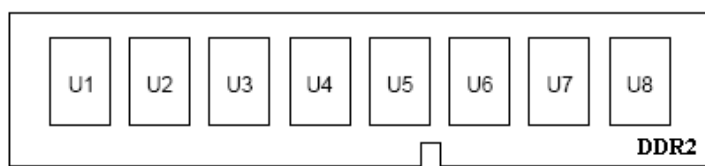
## B-2 Modules with nMx8 Ics

IC pins	Corresponding module pins
U1: 0 → 7	0, 1, 2, 3, 4, 5, 6, 7
U2: 0 → 7	8, 9, 10, 11, 12, 13, 14, 15
U3: 0 → 7	16, 17, 18, 19, 20, 21, 22, 23
U4: 0 → 7	24, 25, 26, 27, 28, 29, 30, 31
U5: 0 → 7	32, 33, 34, 35, 36, 37, 38, 39
U6: 0 → 7	40, 41, 42, 43, 44, 45, 46, 47
U7: 0 → 7	48, 49, 50, 51, 52, 53, 54, 55
U8: 0 → 7	56, 57, 58, 59, 60, 61, 62, 63

If 'ECC chip' setting is selected, the ECC IC(s) are automatically added in the middle of the module, and other ICs are shifted accordingly:

U5: 0 → 7	64, 65, 66, 67, 68, 69, 70, 71 (Parity/ECC)
-----------	---

*Figure B-2.  
Standard 8-Bit IC DIMM Reference  
Designator Map*



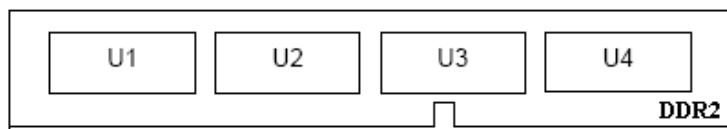
## B-3 Modules with nMx16 Ics

IC pins	Corresponding module pins
U1: 0 → 15	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15
U2: 0 → 15	16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31
U3: 0 → 15	32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47
U4: 0 → 15	48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63

If 'ECC chip' setting is selected, the ECC IC(s) are automatically added in the middle of the module, and other ICs are shifted accordingly:

U3: 0 → 7	64, 65, 66, 67, 68, 69, 70, 71 (Parity/ECC)
-----------	---

*Figure B-3.  
Standard 16-Bit IC DIMM Reference  
Designator Map*



## Appendix C

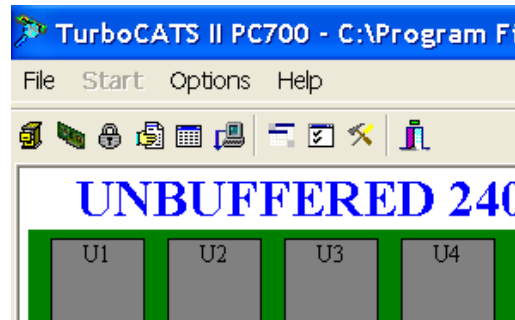
### Sorting Function

#### C-1 Sorting Table Function Description

The TurboCATS II 700MHz DDR Memory Tester has a Sorting Table function for sorting ICs based on the test results. If this function is turned on, then at the end of testing the failed ICs will be displayed using multiple colors and descriptions set by the user before the test. This significantly aids the module repair and IC sorting process. Both bit and address sorting functions are available.

The user must purchase a license in order to use the Sorting Table feature with the TurboCATS testers. We can generate a **license.tc2** file for each tester based on its PC's hard drive serial number (in DOS command prompt screen type '**vol**' to obtain this number). The user must then copy the file to the **C:\Program Files\TCII-700** directory on the PC. The tester and PC software both must be re-started to recognize the license file. A new Sorting Table icon will appear on the software main screen, as shown in *Figure C-1*.

Figure C-1. Sorting Table Icon on Main Screen



#### C-2 Opening Sorting Table File

The Sorting Table function can be enabled/disabled by selecting the **Sorting** setting on the main software screen (see *Figure C-2*). If the **Sorting** setting is not checked, then the test will run as usual without using the Sorting Table function. If the **Sorting** setting is checked, then the test results will be sorted based on the parameters defined in the Sorting Table file opened before running the test (or the default file **Template.st**, if no new file was opened). The Sorting Table file has **.st** extension.

Figure C-2. Sorting Setting on the Main Screen

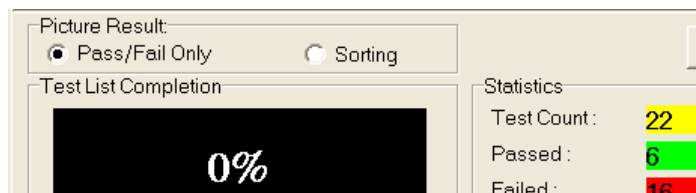




Figure C-4. Sorting Table  
Preview Screen

Priority	Label	Slot	Description	Masked Bits 4/8/16/32 (LSB..MSB)	Failure On
0	ERR	8	Error - address failed		
1	G	8	Good - no bad bit		
2	NF	8	Not Found - type not defined		

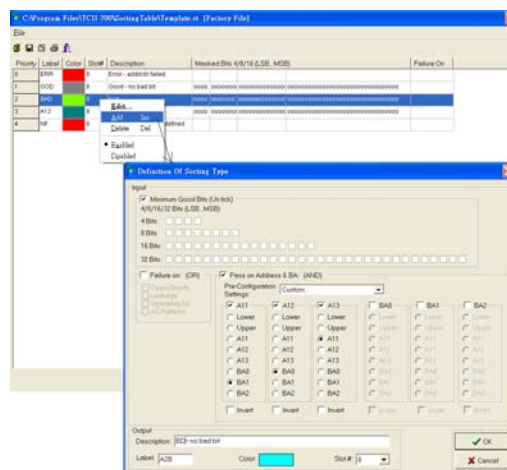
## C-3 Editing Sorting Table File

The Sorting Table file consists of several sorting type entries (or records), which define how the failed ICs will be sorted. Color, descriptions and even the type of failures can be custom-defined by the user.

The order of sorting records determines the failure display priority. For example, if the 1<sup>st</sup> entry in the Sorting Table is “**All Good**”, and the 2<sup>nd</sup> one is “**Upper Half Good**”, then the ICs with all good bits will be selected first at the end of the test, and then the ones with upper half good bits will be selected from the remaining chips. To change the sorting priority of an entry, you can highlight it and drag it to the desired location.

By right-clicking on any highlighted sorting entry, the user can select to **Edit** or **Delete** that entry, or **Enable / Disable** it. Please note that the last sorting entry **NF** cannot be deleted. **NF** stands for all failures, which did not fall into any other categories, and is located at the bottom of the sorting table (lowest priority). **ERR** failure is defined as a control or address line failure, is placed by default at the beginning of the sorting table (highest priority), but can be moved. For the recommended sorting entry order, see **Figure C-5** below. If **Add** function is selected, a new sorting entry will be placed at the bottom of the list before the last **NF** entry. You can also double-click on the highlighted sorting entry to get to its Editor window – see **Figure C-5**.

Figure C-5. Bit Sorting Record Editor Menu



**Minimum Good Bits (Input)**

Defines the selected failure type – unchecked bits have to be good for the IC to qualify under this sorting category. The checked bits are “don’t cares” - they can be either good or bad. The order of the check boxes is from the Least Significant Bit to the Most Significant Bit, for example, DQ0 -> DQ7 for the 8-bit ICs.

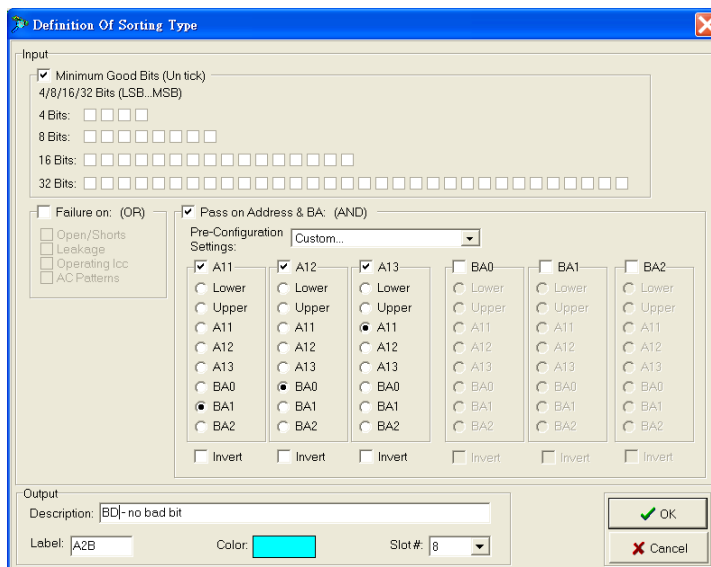
**Failure On (Input)**

The ICs that failed a selected pattern (Open/Shorts, Leakage, Operating ICC, or AC patterns) will qualify under this sorting type. The listed settings can be selected alone or together in any combination.

**Pass on Address & BA (Input)**

The ICs that passed a selected combination of address and BA lines will qualify under this sorting type. The combination of lines can be defined manually or selected from the list of pre-defined address sorting standards (see *Figure C-6*). Note that all Address Sorting records are pre-set to have the same teal color.

Figure C-6. Address Sorting Record Editor Window



<b>Description</b> (Output)	This field holds up to 30 characters, which will show on the sorting table as the record description (for example, " <b>Upper Half Good IC</b> ").
<b>Label</b> (Output)	This label will be displayed on the chip picture itself on the final test result screen. This field can only contain 3 or fewer characters (for example, " <b>UP</b> ").
<b>Color</b> (Output)	The user can select any color of his choice for easier identification of the failed chips. Click on the color field box to get to the color editor window.
<b>Slot #</b> (Output)	This field is used for the IC Sorting Handler.

## C-4 Running Test with Sorting Function

Follow the steps below to run the test with the Sorting Function:

1. On the Main Software Screen click on the Sorting Function icon. Open a desired Sorting Table file, then exit back to the Main Screen.
2. Select the **Sorting** radio button on the Main Screen.
3. Set up your Test File and start testing as usual.

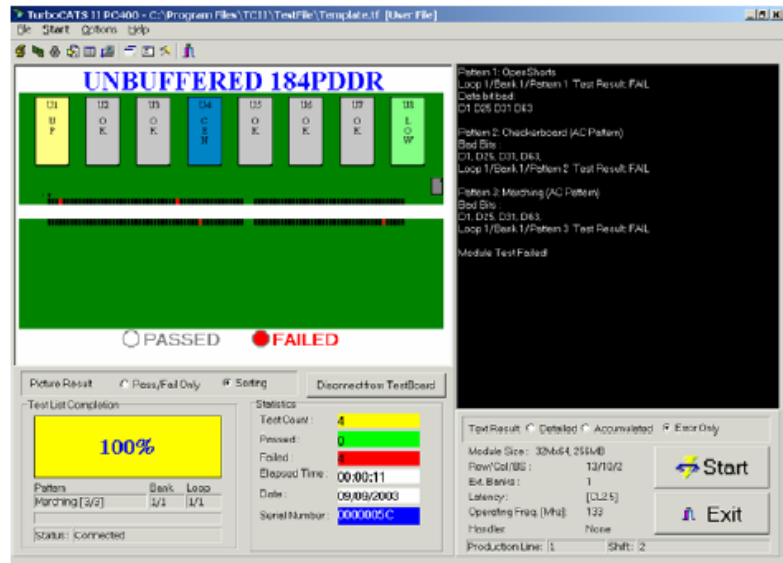
At the end of the test the picture results will be displayed using colors and labels selected in the Sorting Table file for different types of failures. *Figure C-7* below is an example of test results obtained using a Sorting file **Simple Sorting.st** shown previously in *Figure C-5*. Double-click on the picture result window on the Main Screen to get a larger picture of the module as shown. You can zoom in on each individual IC by double-clicking on it (or right-clicking on IC and selecting **zoom+**) – this way you will see the actual bits that failed.

The screenshot shows the TestFlasher 1.0.0.0 application window. The title bar indicates the file path: C:\Program Files\Toshiba\TestFlasher 1.0\Toshiba File. The main window has a green background with the text 'UNBUFFERED 184PDDR' at the top. Below this, there are eight memory modules represented by colored squares: U1 (yellow), U2 (grey), U3 (grey), U4 (red), U5 (grey), U6 (grey), U7 (grey), and U8 (green). The status bar at the bottom shows 'PASSED' in green and 'FAILED' in red. A small window titled 'Picture Result' shows a yellow box with '100%' and a green box with '0%'. The 'Statistics' section shows 'Test Count: 1', 'Passed: 0', 'Failed: 0', 'Elapsed Time: 00:00:10', 'Date: 09/09/08', and 'Serial Number: 00000005'. The 'Patterns' section shows 'Pattern: Marching (AC Pattern)', 'Bank: 1/2', and 'Loop: 1/1'. The 'Status' section shows 'Connected'. A detailed test log on the right shows three patterns (Open Short, Checkboard, and Marching) all passing. A smaller window at the bottom right shows a close-up of the memory module with a yellow label 'U1 U P' and '32MB 184PDDR'.

### Figure C-8. Extensive Sorting Table

Priority	Label	Color	Slot#	Description	Masked Bits 4/6/16 LSB -MSG	Failure On
0	AC	Orange	0	addressed control line failure		
1	OK	Grey	1	all good bits	0000 00000000 0000000000000000 00000000000000000000000000000000	
2	UP	Yellow	2	upper half good	0000 00000000 0000000000000000 00000000000000000000000000000000	
3	LOW	Green	3	lower half good	0000 00000000 0000000000000000 00000000000000000000000000000000	
4	WPL	Cyan	4	split bits good	0000 00000000 0000000000000000 00000000000000000000000000000000	
5	CDN	Blue	5	center bits good	0000 00000000 0000000000000000 00000000000000000000000000000000	
6	EVC	Pink	6	even bits good	0000 00000000 0000000000000000 00000000000000000000000000000000	
7	ODD	Purple	7	odd bits good	0000 00000000 0000000000000000 00000000000000000000000000000000	
8	RAO	Red	8	type not found above - load IC		

Figure C-9. Extensive Sorting Results



Bit D1 failed → U1 is sorted as a Lower Half Good IC (yellow).

Bits D25 & D31 failed → U4 is sorted as a Center Bits Good IC (blue).

Bit D63 failed → U8 is sorted as Upper Half Good IC (green).

STOP AT FAILURE function inside the Test File should be set to OFF when running the sorting test.



**NOTE:** If running data bit sorting, the first entry (highest priority) in Sorting Table files should be the Address/Control Line Failure (see **Simple Sorting.st** and **Extensive Sorting.st** files as examples). If at the end of the test all your ICs are labeled A/C, that means one or more of the address or control lines are shorted. In this case the user needs to look at the text result to determine which line failed and run Leakage test to figure out what IC might be causing the problem. The bad IC should be removed and the rest of the ICs should be retested using a regular sorting file. If one or more of the Address or Control lines are open, the software can actually determine which IC is causing the problem and will only highlight that IC.